Lab 3

ENGR 2323

Digital Design Lab

Class Outline

- Combinational circuit design.
- Circuit realization using discrete logic.
- Datasheets.
- Annotating Quartus Schematics.
- Circuit Implementation and testing.
- Lab 3 deliverables.

Objectives

- Be able to simplify Boolean expressions using Karnaugh maps.
- Be able to realize Boolean expressions using mixed logic and create the schematic using Intel Quartus CAD software.
- Be able to obtain device and pin information from integrated circuit manufacturer datasheets.
- Be able to realize and test digital circuits using discrete logic (SSI gates), a solderless protoboard, and a powered protoboard.

Important Terms/Concepts

- Small to medium designs and prototypes are often realized using discrete-logic. Solderless protoboards allow for prototyping with little to no special equipment.
- Important terms/concepts include:
  - Discrete logic
  - Datasheet
  - Solderless protoboard

Combinational Circuit Design

- Combinational circuit design involves designing and implementing a circuit that operates according to set of specifications.
- The specifications may be a formal description such as a function table or Boolean expression(s) or it may be informal such as a problem description. Informal descriptions are often incomplete.
- The combinational circuit design process for small to mid-size designs typically involves:
  - creating a function table
  - generating logic expressions for each output (often will simplify the expression)
  - Implementing (building) the circuit
  - Verifying the circuit operation

Karnaugh Maps

- Karnaugh maps are a graphical method of simplifying Boolean expression. Karnaugh maps work well when have five or fewer variables in the expressions.
- To simplify a Boolean expression using Karnaugh maps:
  - Form the Karnaugh map.
  - Group the ones for a MSOP. Make sure to use as large of groups as possible and reuse ones if it allows a larger group.
  - Variables with the same value in the group are kept. Variables whose value changes in the group are dropped.
  - Write a simplified minterm for the variables that are kept.
  - Sum the minterms to obtain the MSOP.

Simplification using Karnaugh Maps

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 1. Truth Table

$$F = \sum_{ABCD} (1,3,4,5,6,7,9,10)$$

AB/CD	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	0	0	0	0
10	0	1	0	1

Figure 2a. Karnaugh Map

Simplification using Karnaugh Maps

AB/CD	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	0	0	0	0
10	0	1	0	1

$\bar{A} \cdot D$

$\bar{A} \cdot B$

$\bar{B} \cdot \bar{C} \cdot D$

$A \cdot \bar{B} \cdot C \cdot \bar{D}$

Figure 2b. Karnaugh Map with Groups

Two groups of four, one group of two,
one group of one

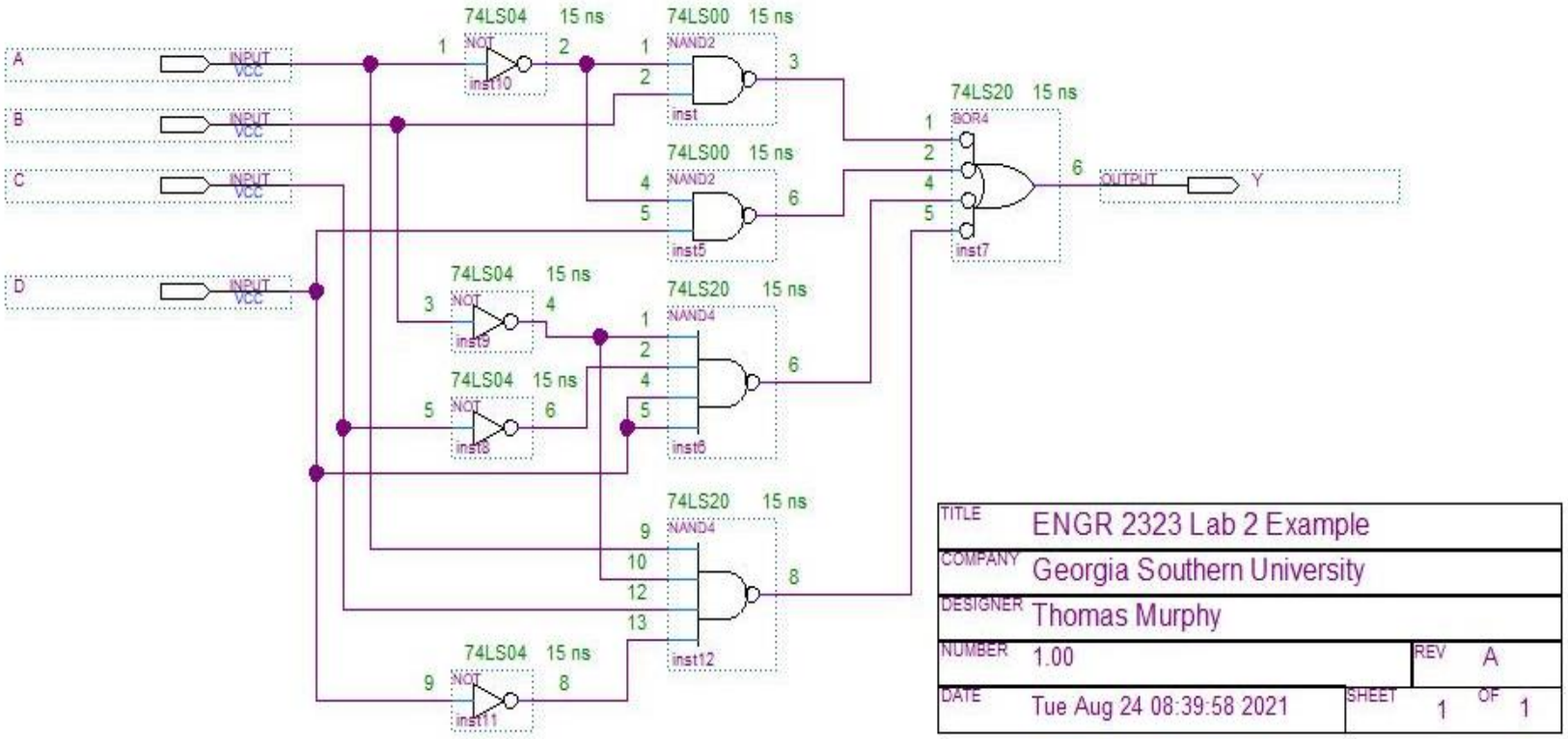
$$F = \bar{A} \cdot B + \bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot D + A \cdot \bar{B} \cdot C \cdot \bar{D}$$

Realizing MSOP Expressions

- MSOP requires two AND2, one AND3, one AND4, and one OR4 operation. Also four NOT operations.
  - Use NAND2 for the AND2 operations, NAND4 for the AND3 and AND4 operations. Tie unused input pins to a duplicate of one of the inputs.
  - Use bOR4 (NAND4) for the OR4 operation.

$$F = \bar{A} \cdot B + \bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot D + A \cdot \bar{B} \cdot C \cdot \bar{D}$$

Realizing MSOP Expressions

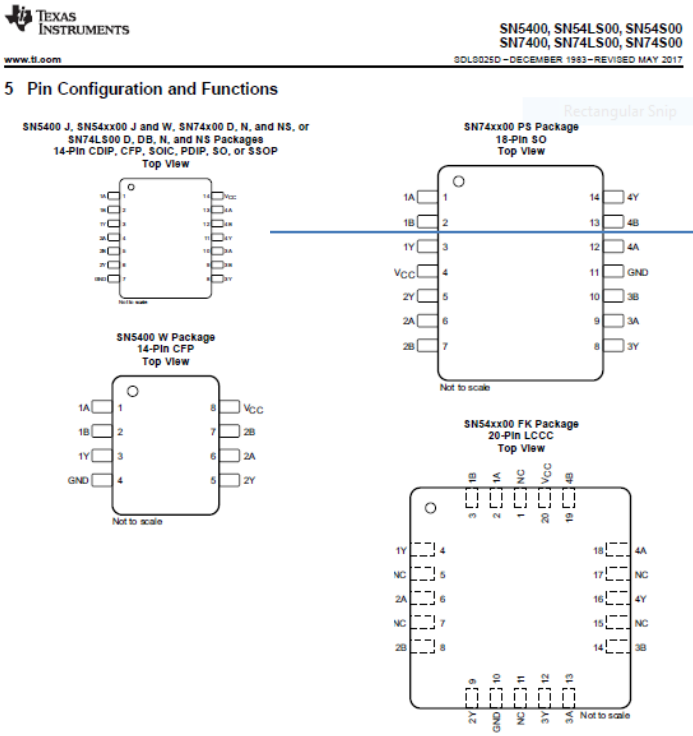


$$F = \overline{A} \cdot B + \overline{A} \cdot D + \overline{B} \cdot \overline{C} \cdot D + A \cdot \overline{B} \cdot C \cdot \overline{D}$$

Datasheets

- You will need datasheets for the following discrete logic chips: 74LS00, 74LS04, and 74LS20.
- These devices will be used to realize your design and the datasheets will specify the pin connections for the discrete logic. All parts of a given type, for example all LS00, have the same specifications regardless of manufacturer but some manufacturers have easier to read datasheets than others.
- Links for Texas Instruments and ON Semiconductor websites for obtaining data sheets are (we are using LS series devices):
  - Texas Instruments: http://www.ti.com/
  - ON Semiconductor: http://www.onsemi.com/

SN74LS00 Datasheet



TEXAS INSTRUMENTS
www.ti.com

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
SDLS025D – DECEMBER 1983 – REVISED MAY 2017

5 Pin Configuration and Functions

SN5400 J, SN54xx00 J and W, SN74x00 D, N, and NS, or SN74LS00 D, DB, N, and NS Packages
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP
Top View

SN74xx00 PS Package
18-Pin SO
Top View

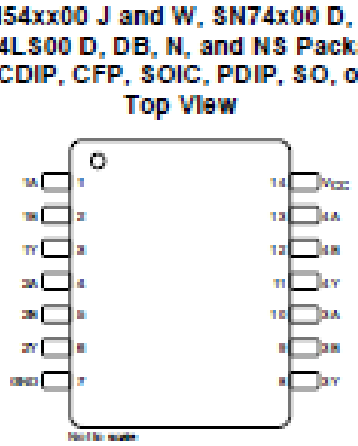
SN5400 W Package
14-Pin CFP
Top View

SN54xx00 FK Package
20-Pin LCCC
Top View

Not to scale

Pin Functions

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
1A	1	1	1	2	I	Gate 1 Input
1B	2	2	2	3	I	Gate 1 Input
1Y	3	3	3	4	O	Gate 1 output
2A	4	6	6	6	I	Gate 2 Input
2B	5	7	7	8	I	Gate 2 Input
2Y	6	5	5	9	O	Gate 2 output
3A	10	—	9	13	I	Gate 3 Input
3B	9	—	10	14	I	Gate 3 Input



DIP configuration, Vcc is pin 14, GND is pin 7, first NAND2 is pins 1, 2, and 3, etc.

The pin configuration can usually be found on one of the first few pages. For example, the Texas Instruments 74LS00 datasheet has the pin configuration on page 3.

Annotating Quartus Schematics

- Schematics can be annotated in Quartus using the text tool (upper case A in schematic toolbar).
- Select the location to add text and type in the text. The annotations from the text tool are objects that can be grabbed and moved around.
- Make sure the annotations are clear and do not block devices or wires. This may require rearranging your circuit.

Circuit Implementation

- Remember to use only devices in your discrete logic chipset for your circuit design (NAND2, NAND4, NOT).Follow proper mixed logic.
- Make sure you get the datasheet for the correct logic family (LS).
- Annotate your schematic before starting to build your circuit so you have a connection guide.

Circuit Implementation

- Make sure to press the integrated circuits firmly into the solderless protoboard.
- Make sure to connect power and ground to every integrated circuit
- Keep the circuit organized and wires as short as possible. Try to avoid having wires crossing other wires or going over integrated circuits.
- Label your inputs and outputs of the circuit so you can hook your circuit to the CADET board’s switches and LEDS correctly.
- You will also use the same circuit next week for Lab 4 and will need to be able to connect it up again.

Circuit Testing

- Make sure you know what the design you testing is supposed to do, i.e. be able to compare the operation to or a function table, logic expressions, or simulation waveforms.
- Make sure to test the circuit for all input combinations; for 4 variables there are 16 combinations: 0000, 0001, … 1110, 1111.

Lab 3 Deliverables

- Lab 3 Prelab
  - Function table, solved Karnaugh map indicating groups and terms, and the MSOP expression for the circuit output. A template has been provided for formatting function tables and Karnaugh maps.
  - Quartus schematic for the design.
  - Functional simulation results.
- Lab 3 Work
  - Determine the integrated circuit pin numbers for the inputs and outputs of each gate in your circuit design using the discrete logic chip datasheets.
  - Annotate the Quartus schematic with the device pin numbers you will use to build the circuit.
  - Constructed circuit.
  - Verify the circuit operation.
- Lab 3 Results
  - Function table, solved Karnaugh map indicating groups and terms, and the MSOP expression for the circuit output.
  - Annotated Quartus schematic for the design.
  - Functional simulation results.
  - Image (appropriately cropped) of the constructed circuit.
  - Explanation of how the realized circuit operation was verified.