Lab 5

ENGR 2323

Digital Design Lab

Class Outline

- Sequential circuit (state machine) design.
- Flip-flop operation.
- Sequential circuit testing.
- Lab 5 deliverables.

Objectives

- Be able to design a state machine given a state machine transition table.
- Be able to create state diagrams corresponding to a state machine transition table.
- Be able to realize a state machine design and create the schematic using Intel Quartus CAD software.
- Be able to realize and test digital circuits using discrete logic (SSI gates), a solderless protoboard, and a powered protoboard.

Important Terms/Concepts

- Sequential circuits have memory elements combined with combinational logic. The memory elements can be individual flip-flops/latches, registers, or larger memory elements depending on the design complexity.
- The sequential circuit design process allows the design of circuits that rely on past information about the inputs such as counters, sequence generators, and sequence recognizers.
- Important terms/concepts include:
  - sequential circuit (state machine)
  - clock, synchronous
  - state, state memory
  - state transition table, state diagram
  - next state equations, output equations

Sequential Circuit Design

- Starting with the state transition table:
  - Create the state diagram (typically this is done from a problem statement before the state transition table is created).
  - Determine the next state and output expressions. Remember that the output is a function of the current state not the next state.
  - Simplify the expressions (MSOPs) if the design will be realized using SSI gates. Make sure you take advantage of the don't cares when simplifying the next state and output equations.
- Once the next state and output equations are determined, realize the design. For a discrete logic realization:
  - Use a bank of flip-flops for the state memory.
  - Next state equations circuit is a combinational circuit providing flip-flop input for the state transition based on current state and current input.
  - Output equation circuit is a combinational circuit providing the output based on current state and current input (for this lab, the output will only depend on the state).

Design of a Modulo 3 Counter

- Module 3 counter counts 0, 1, 2, 0, etc. There are three states so 2-bits of state memory and two state variables are needed.

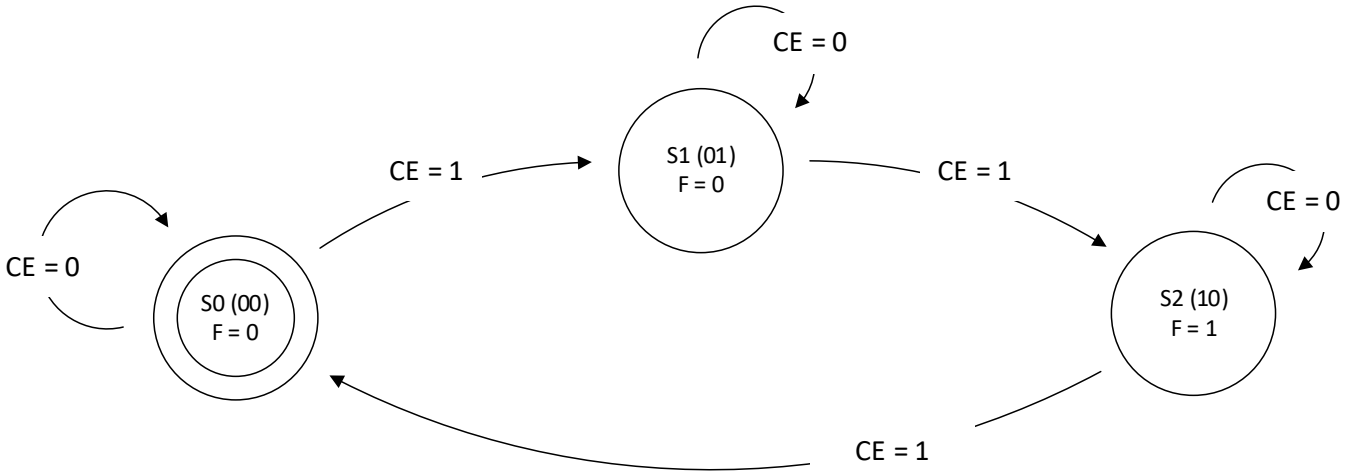


Figure 1. State Diagram of Modulo 3 Counter

Design of a Modulo 3 Counter

- State transition table will have one row for each state-input combination in the state diagram.

Q1 Q0	CE	Q1+ Q0+	F
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 1	0
0 1	1	1 0	0
1 0	0	1 0	1
1 0	1	0 0	1
1 1	0	DC DC	DC
1 1	1	DC DC	DC

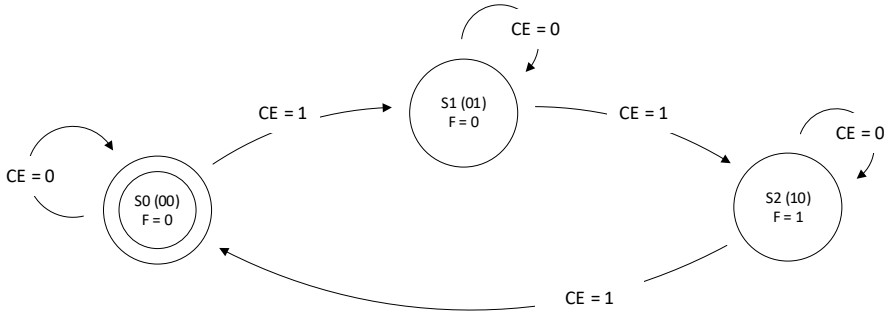


Figure 2. State Transition Table of Modulo 3 Counter

Design of a Modulo 3 Counter

Simplified next state and output expressions

Q1/Q0 CE	00	01	11	10
0	0	0	1	0
1	1	0	X	X

$$Q_1^+ = Q_1 \cdot \overline{CE} + Q_0 \cdot CE$$

Q1/Q0 CE	00	01	11	10
0	0	1	0	1
1	0	0	X	X

$$Q_0^+ = \bar{Q}_1 \cdot \bar{Q}_0 \cdot CE + Q_0 \cdot \overline{CE}$$

Q1/Q0 CE	00	01	11	10
0	0	0	0	0
1	1	1	X	X

$$F = Q_1$$

Design of a Modulo 3 Counter

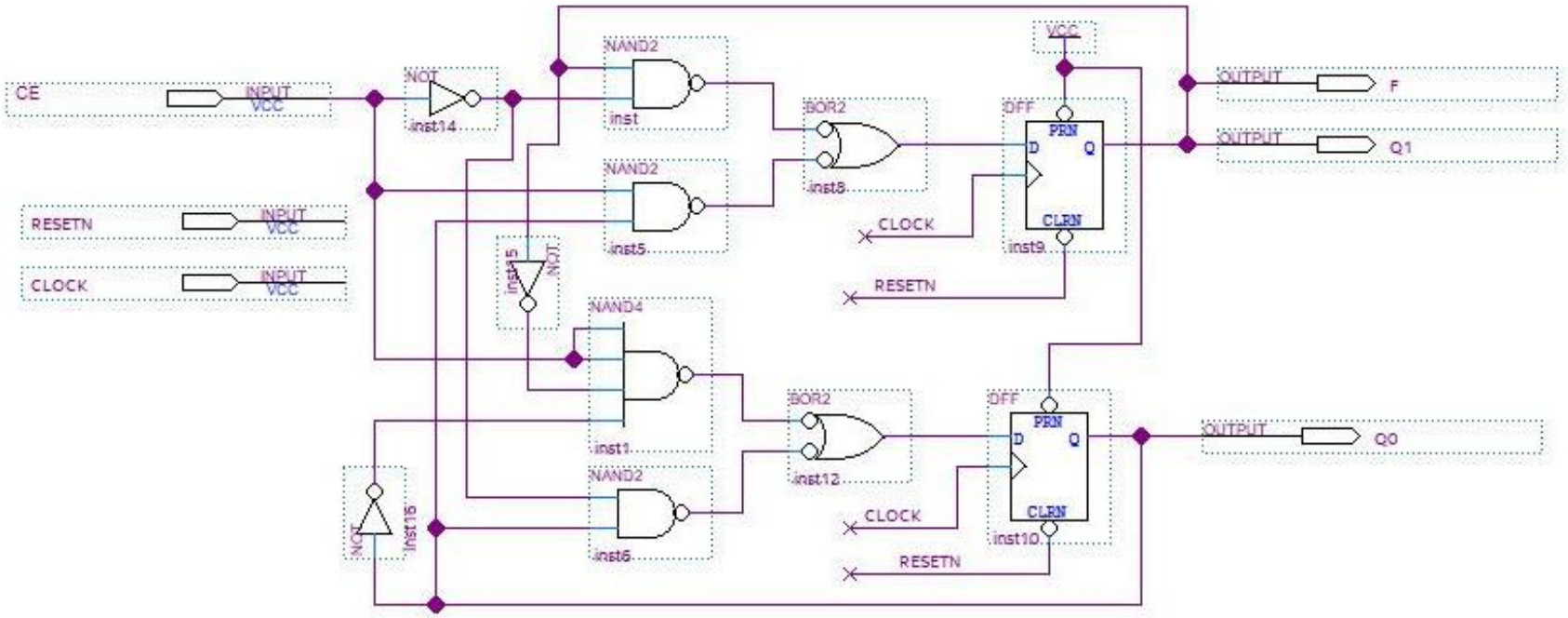


Figure 3. Schematic for Modulo 3 Counter

$$D_1 = Q_1^+ = Q_1 \cdot \overline{CE} + Q_0 \cdot CE$$

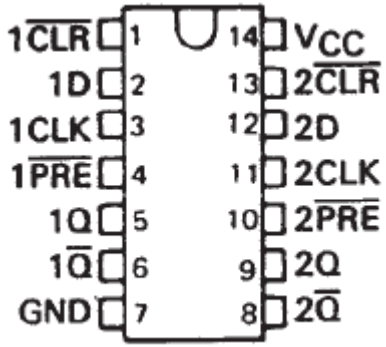
$$D_0 = Q_0^+ = \bar{Q}_1 \cdot \bar{Q}_0 \cdot CE + Q_0 \cdot \overline{CE}$$

$$F = Q_1$$

Note that CLOCK and RESETN are connected to the D flip-flops using virtual connections. The D flip-flop presets are deactivated.

D Flip-flop Operation

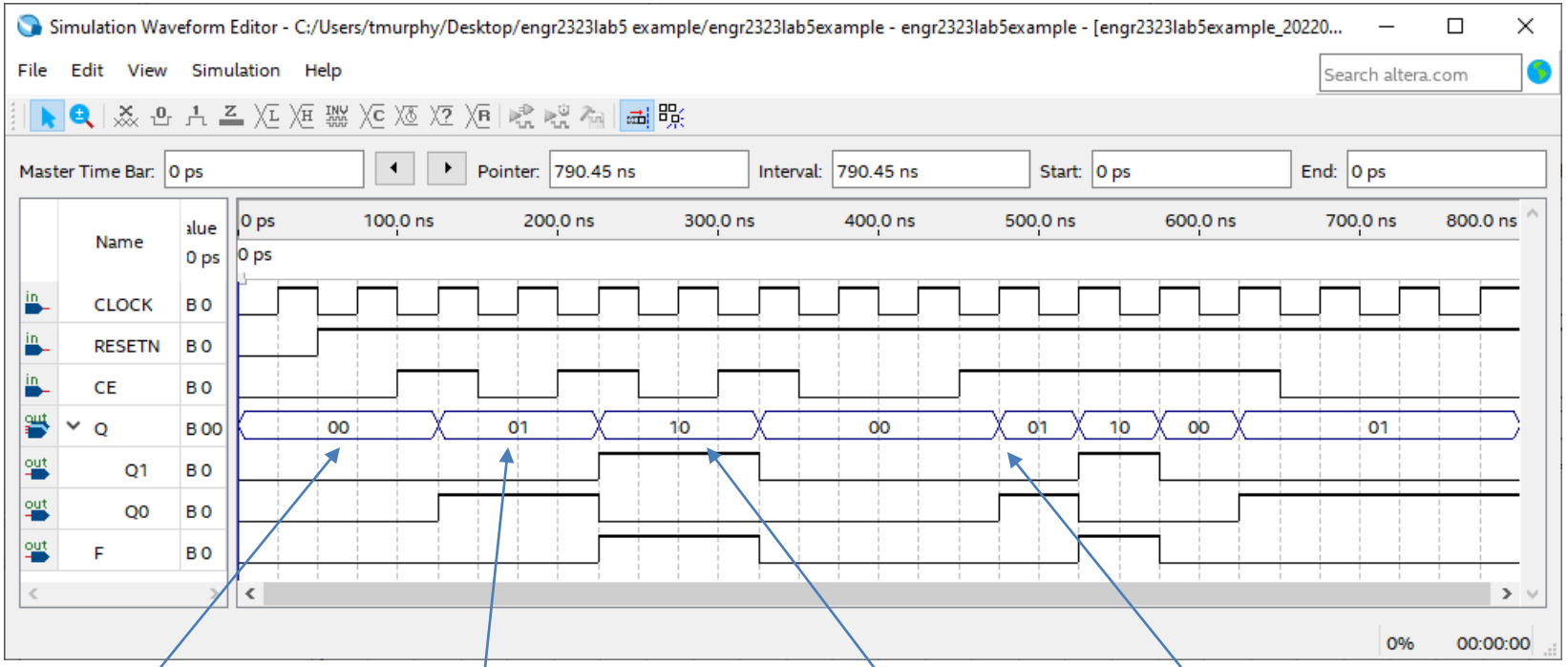
- Flip-flops are edge triggered memory devices. As long as the flip-flop has power it will store the value.
- On the active edge of the clock (rising edge for 7474), the flip-flop will read in whatever is on its D input and that will be the new stored value.
- Most flip-flops have a direct clear and direct preset. Activating the clear or preset will set the flip-flop to 0 or 1 respectively. We will not be using the preset in lab so that input should be deactivated (set to high since it is active low.



Sequential Circuit Testing

- To fully test a sequential circuit, all input combinations for each state must be verified. This can be difficult and very tedious as it is not always easy to put the sequential circuit in the desired state to test.
- For a counter type design, this is not as problemsome since when counting the circuit cycles through all its states. To test the counter:
  - Rest the circuit to State 0, test inputs 0 and 1, input of 1 will take us to state 1
  - With circuit in State 1, test inputs 0 and 1, input of 1 will take us to state 2
  - With circuit in State 2, test inputs 0 and 1, input of 1 will take us to state 0
  - It is also helpful to have a sequence illustrating normal operation, in this counting from 0 to 2 and rolling over.
- For more complex designs where the state diagram is not a ring or line of states, it is often more practical to determine a sequence of inputs that causes the circuit to go through all its state-input combinations but not necessarily in the same order as the state transition table. That is how we will test the circuit designed in lab 5.

Testing Modulo 3 Counter



Test S0, CE = 0, 1

Test S1, CE = 0, 1

Test S2, CE = 0, 1

Test counting

Note the state variables Q1 and Q0 are grouped for easier reading

Sequential Circuit Testing

- To test the constructed sequential circuit:
  - The reset and clock will come from a pushbutton with pull up resistor.
  - Reset the circuit using the reset placing it in state Q1Q0 = 00
  - Set the input X1X0 using the slide switches for the first transition, push the button for the clock. Verify that the next state is correct. Verify the output is correct for the state.
  - Repeat the process of setting the input X1X0 using the slide switches, activating the clock, and verifying the next state for each input combination in the functional simulation.

Lab 5 Deliverables

- Lab 5 Prelab
  - State transition table, state diagram, solved Karnaugh maps indicating groups and terms for next state and output expressions, and the MSOP expressions for the circuit next state and output expressions.
  - Quartus schematic for the state machine design.
  - Functional simulation results for the design.
- Lab 5 Work
  - Determine the integrated circuit pin numbers for the inputs and outputs of each gate in your circuit design using the discrete logic chip datasheets.
  - Annotate the Quartus schematic with the device pin numbers you will use to build the circuit.
  - Constructed circuit.
  - Verify the circuit operation.

Lab 5 Deliverables

- Lab 5 Results
  - State transition table, state diagram, solved Karnaugh maps indicating groups and terms for next state and output expressions, and the MSOP expressions for the circuit next state and output expressions.
  - Annotated Quartus schematic with device and pin labels for the design.
  - Functional simulation results for the design.
  - Image (appropriately cropped) of the constructed circuit.
  - Explanation of how the realized circuit operation was verified.