ENGR 2323 Digital Design Lab
Lab 3 Realizing Combinational Circuits using Discrete Logic

Introduction

A 4-input 1-output combinational circuit will be designed, realized, and tested. The minimum sum of products (MSOP) expression for the design will be realized using a solderless protoboard and discrete logic. The circuit will be tested using a powered protoboard.

Objectives

After completing this lab students should:

1. Be able to simplify Boolean expressions using Karnaugh maps.
2. Be able to realize Boolean expressions using mixed logic and create the schematic using Intel Quartus CAD software.
3. Be able to obtain device and pin information from integrated circuit manufacturer datasheets.
4. Be able to realize and test digital circuits using discrete logic (SSI gates), a solderless protoboard, and a powered protoboard.

Background

1. Combinational Circuit Design document (Readings)
2. Solderless Protoboard with Circuit Built video (Readings)

Lab 3 Prelab

For the provided lab 3 function table:

- Using a Karnaugh map, determine the MSOP expression for the circuit output F.
- Create a Quartus project and enter the design using the schematic editor. The schematic of the design should have a title block.
- Compile and simulate the design (functional simulation) for all sixteen input combinations.
- Verify the design operation using the simulation results.
- Obtain datasheets for the following discrete logic chips: 74LS00, 74LS04, and 74LS20.

Lab 3

Determine the integrated circuit pin numbers for the inputs and outputs of each gate in your circuit design using the discrete logic chip datasheets.

Using the Quartus schematic editor, annotate the circuit with the device chip names (74LSXX) and annotate the inputs and outputs of each gate with the device chip pin numbers.
pin numbers. The result should look something like Figure 1. Note in mixed logic, a positive logic NAND gate such as the 75LS20 in Figure 1 that is used to perform a logical OR operation is shown as a bOR gate.

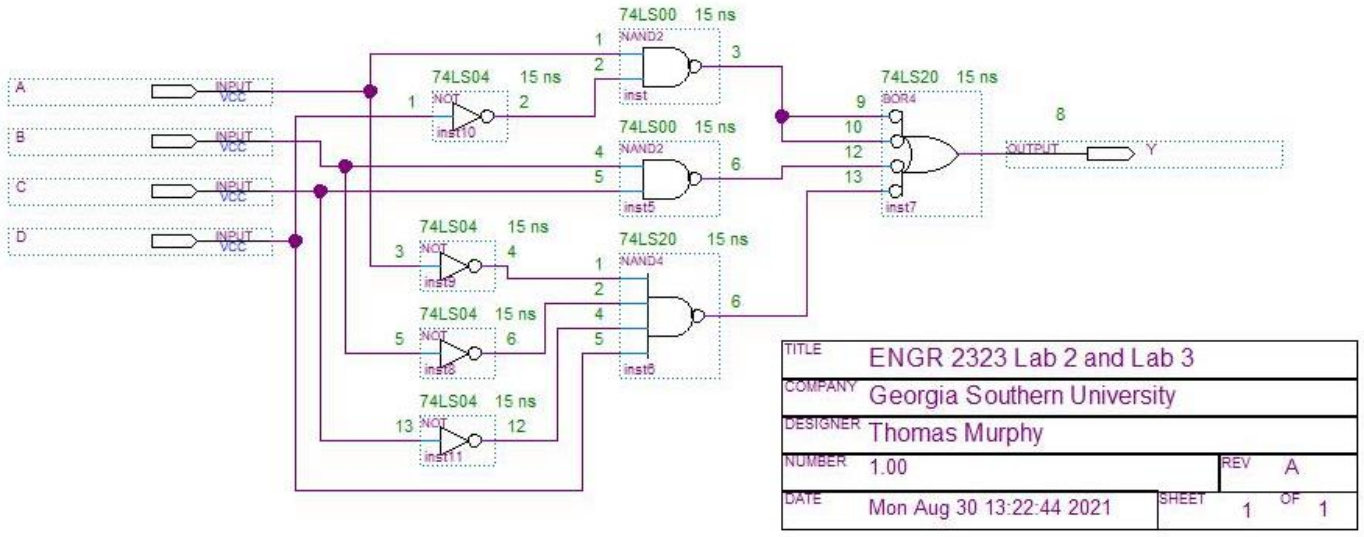

Figure 1. Annotated Schematic with Device and Pin Labels

Using the annotated schematic, construct your circuit on a solderless protoboard. Remember that besides the gate pin connections, each integrated circuit will also need power and ground connections which are typically pins 7 and 14 on 14-pin dual inline package chips (14-pin DIP). Make sure that you have labeled or used color-coded wires for the circuit inputs and outputs.

Connect the powered protoboard switches 1 through 4 (switch 1 to LSB of input and switch 4 to MSB of input) to the circuit inputs and connect the circuit output to one of the LEDs.

Using the powered protoboard, verify the operation of the circuit, and demonstrate the circuit operation to the instructor. To verify the operation, test the circuit for each of the sixteen input combinations and ensure they match the simulation results and circuit function table.

Take a picture of your constructed circuit showing one of the input combinations for which the output is 1 (output LED is lit). Make sure the lighting and contrast are good.

Lab 3 Deliverables

Lab 3 Prelab

Prelab submissions should be Microsoft Word documents and include the prelab work formatted appropriately (use the ENGR 2323 results template).

1. Function table, solved Karnaugh map indicating groups and terms, and the MSOP expression for the circuit output (use the ENGR 2323 function table and Karnaugh map template).

2. Quartus schematic for the design.

3. Functional simulation results for the design.

Lab 3 results
Lab result submissions should be Microsoft Word documents and include the lab work formatted appropriately (use the ENGR 2323 results template).

1. Function table, solved Karnaugh map indicating groups and terms, and the MSOP expression for the circuit output.

2. Annotated Quartus schematic with device and pin labels for the design.

3. Functional simulation results for the design.

4. Image (appropriately cropped) of the constructed circuit.

5. Explanation of how the realized circuit operation was verified.

References
None

Last modified Thursday, August 18, 2022