GEORGIA SOUTHERN UNIVERSITY

ENGR 2323 Digital Design Lab
Lab 7 Design of a Practical Sequential Circuit

Introduction

A modulo-10 up and down counter will be designed, realized, and tested. The counter will be described using VHDL and implemented and tested using a DE10-Standard FPLD development board. The count will be displayed using one of the seven-segment displays on the DE10-Standard board.

Objectives

After completing this lab students should:

1. Be able to design sequential circuits using a hardware description language such as VHDL.
2. Be able to design and implement a practical sequential circuit using VHDL.
3. Be able to display circuit outputs using a 7-segment display.
4. Be able to explain how clock division is performed and used for implementation of sequential circuits.
5. Be able to verify sequential circuit design operation using simulations and testing on a FPGA development board.

Background

1. Counters and Clock Division document (add link)
2. 7-segment Display document (add link)

Lab 7 Prelab

Design a Modulo-10 up and down counter:

- Develop an algorithm or state diagram for the behavior of a modulo-10 up and down counter. This needs to be detailed enough so that a behavioral VHDL architecture could be developed from it. This will not be turned in, so it only needs to be neat enough for you to read.
- Create a Quartus project and enter the design for the modulo-10 up and down counter using a behavioral VHDL design of the style of Figure 3 of the Counters and Clock Division background document. The inputs for the design should be the clock, reset (active low), count enable, and up/down indication (UDN = 0 to count down and 1 to count up). The output for the design should be the 4-bit count signal. The design will need ten states for the counts from 0 to 9. The design should target the Cyclone V chip on the DE10-Standard board.
- Compile the design and make sure there are no errors.
- Perform a functional simulation of the design. The simulation input should match that of Figure 1. For the output group F, the radix can be changed to an unsigned integer by right clicking on the signal F and from properties, change the radix to unsigned integer. This makes the simulation easier to follow.
- Verify the design operation using the simulation results.

Bring the entire Quartus design project folder and your prelab work to lab.

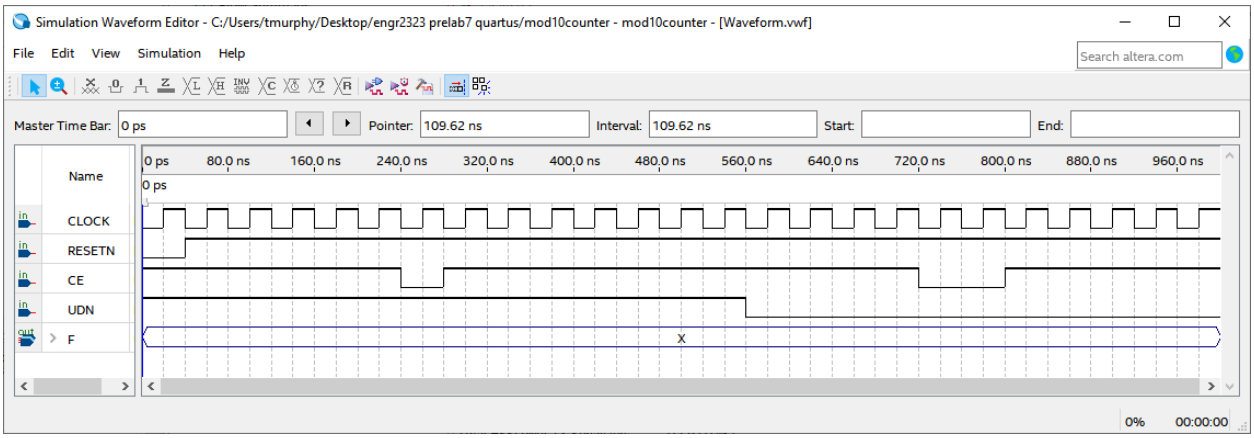

Figure 1. Functional Simulation Waveform

Lab 7

Open your Quartus project from the prelab. Open the VHDL design if it did not open automatically. You will modify the design so that the count can be displayed on a 7-segment display and so that the clock frequency for the counter is 1Hz (count every second).

Add a VHDL description to your design of an appropriate clock divider that will take the 50MHz DE10-Standard clock and provide a 1Hz clock for the counter. Modify the counter portion of the design to use the 1Hz clock.

Add a VHDL description to your design that will convert the count to the appropriate signals to display the count on a 7-segment display. You will need to modify the entity of the design to include the seven signals HEX[6] to HEX[0] for driving the 7-segment display.

Recompile the design and make sure there are no errors, and the project device assignment is correct for the DE10-Standard board.

Using the pin planner, assign pins for the inputs and outputs of the design according to Table 1. The pin assignments corresponding to the DE10-Standard devices can be found in the DE10-Standard Pin Assignments document. The Key inputs are the DE10-Standard pushbuttons. Make sure to also set the FPGA unused pins as inputs tri-stated.

Signal	**DE10-Standard Device**
CLOCK	CLOCK_50
RESETN	Key[3]
CE	SW[1]
UDN	SW[0]
HEX[6..0]	HEX0 7-segment display

Table 1. Input and Output Assignments for Counter

Recompile the design and make sure there are no errors, and the pin assignments are correct.

Program the DE10-Standard board FPGA with your design. Refer to Programming DE10-Standard Board document.

Verify the operation of the counter by resetting the counter, having it count up through the sequence and roll over, count down through the sequence and roll over, and stop the count at a few count values.

Demonstrate the circuit operation to the instructor once you have verified its operation.

Take a picture of the DE10-Standard board showing one of the counts on the 7-segment display.

Next comment out the architecture of your modulo-10 counter design. Create a new behavioral VHDL architecture using the style of Figure 4 of the Counters and Clock Division background document. Do not modify the entity of the design so that the previous pin assignments are preserved. The new architecture can be for a modulo-10 up counter instead of an up and down counter like the previous design.

Recompile the design and make sure there are no errors, and the pin assignments are correct.

Program the DE10-Standard board FPGA with your design.

Verify the operation of the counter and demonstrate the circuit operation to the instructor once you have verified its operation.

Lab 7 Deliverables

Lab 7 Prelab

Prelab submissions should be Microsoft Word documents and include the prelab work formatted appropriately (use the ENGR 2323 results template).

1. Behavioral VHDL design for modulo-10 up and down counter.

2. Functional simulation results for the design.

Lab 7 results

Lab result submissions should be Microsoft Word documents and include the lab work formatted appropriately (use the ENGR 2323 results template).

1. VHDL design for modulo-10 up and down counter including clock divider and 7-segment display modifications.

2. Functional simulation results for the original design from the prelab.

3. VHDL design for modulo-10 up and down counter using the alternative architecture.

4. One image of DE10-Standard board showing a count on the 7-segment display.

5. Explanation of how the two designs' operation was verified on the DE10-Standard board.

References
None

Last modified Wednesday, October 5, 2022