ENGR 2323 Digital Design Lab
Quartus VHDL Designs

Following are the steps to create an Intel Quartus project and enter a design using VHDL. The specific design referred to in this document is a 4-1 multiplexer.

Creating a Quartus Project

Create a Quartus project for the design and save the project in a folder (for example, Lab 2). The project should have a meaningful name such as lab2. The device assignment is the same as used in Lab 1, Cyclone V 5CSXFC6D6F31C6.

Once the project is created, click on “File”, under the Menu Bar, then click on “New”. Under new, click on “VHDL File” as shown in Figure 1.

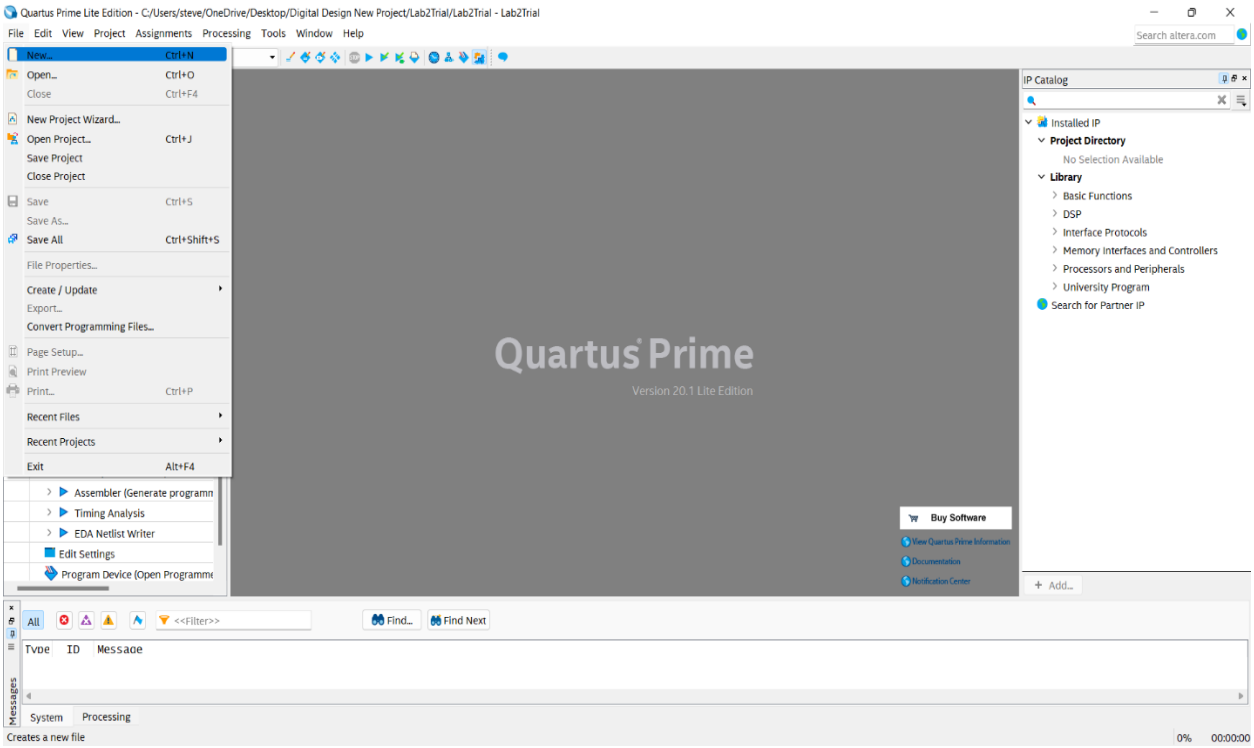

Figure 1. Creating a New Design File

Under new, click on “VHDL File” as shown in Figure 2.

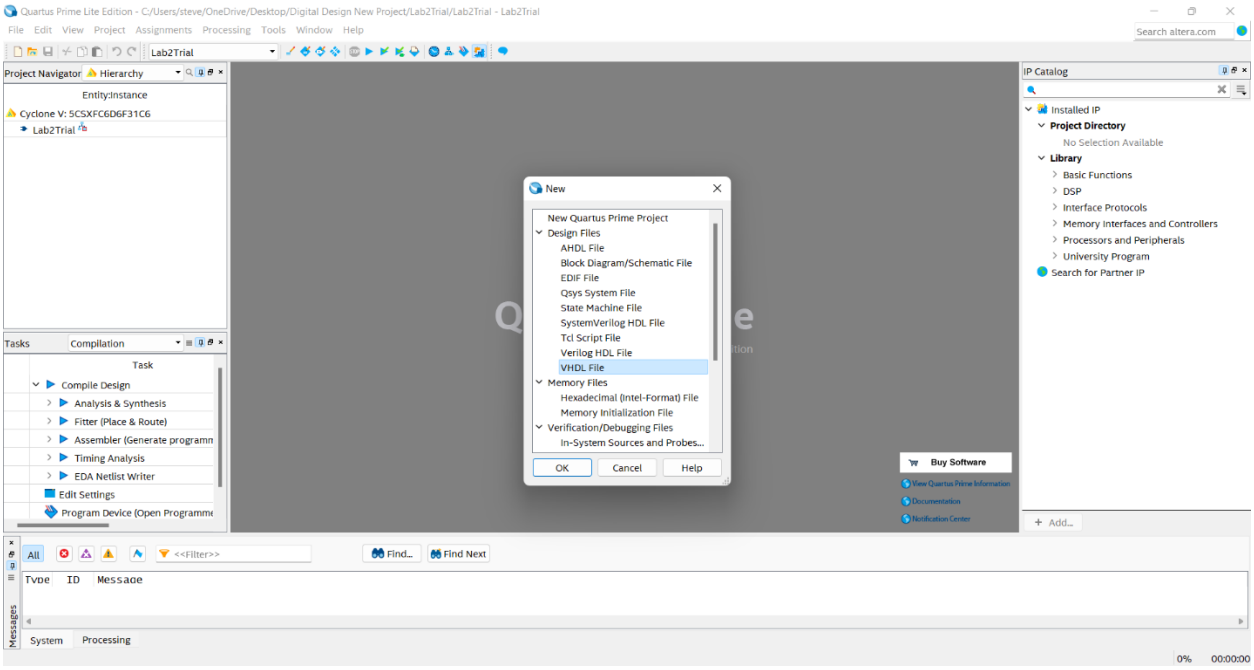

Figure 2. Selecting New VHDL File

Click “OK”. Your Quartus screen should now look like Figure 3.

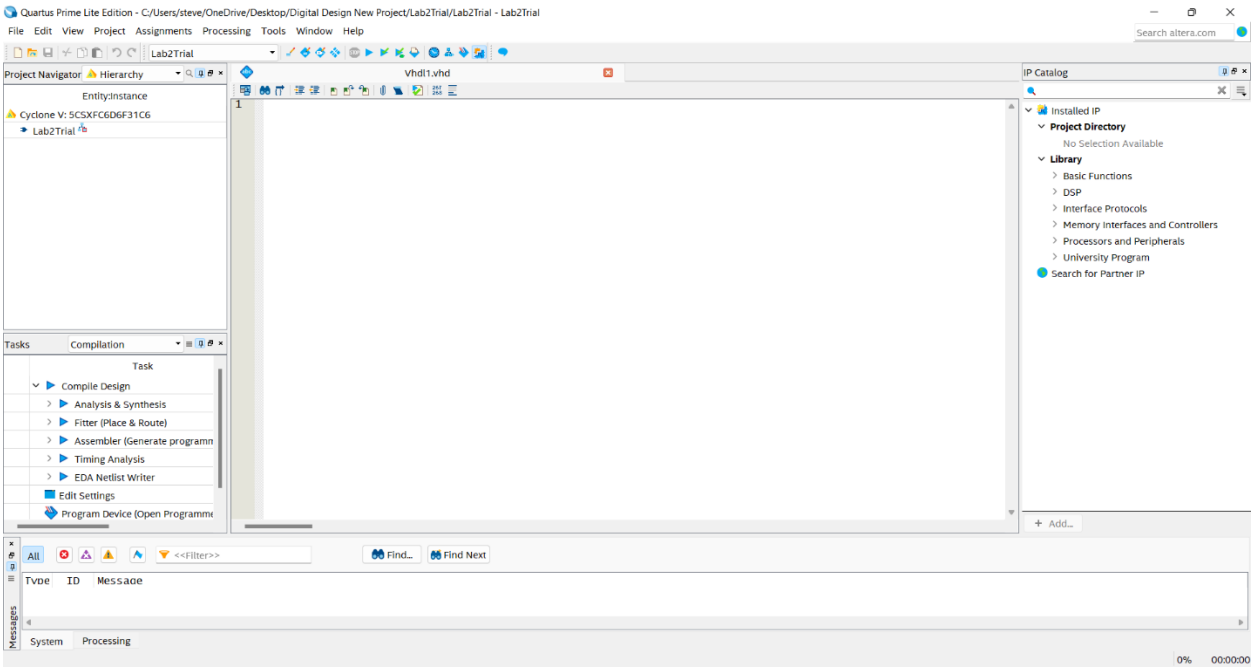

Figure 3. Quartus IDE with VHDL Design File

Make sure the Quartus project name and top-level design file name are the same. For VHDL files, make sure the entity name and filename are the same.

Creating a 4-1 Multiplexer using VHDL

Now you are ready to enter your 4-1 multiplexer design using VHDL and the Quartus editor. The schematic for a 4-1 multiplexer is shown in Figure 4. Determine the logic expression for the output Y as a function of the inputs S1, S0, X3, X2, X1, and X0.

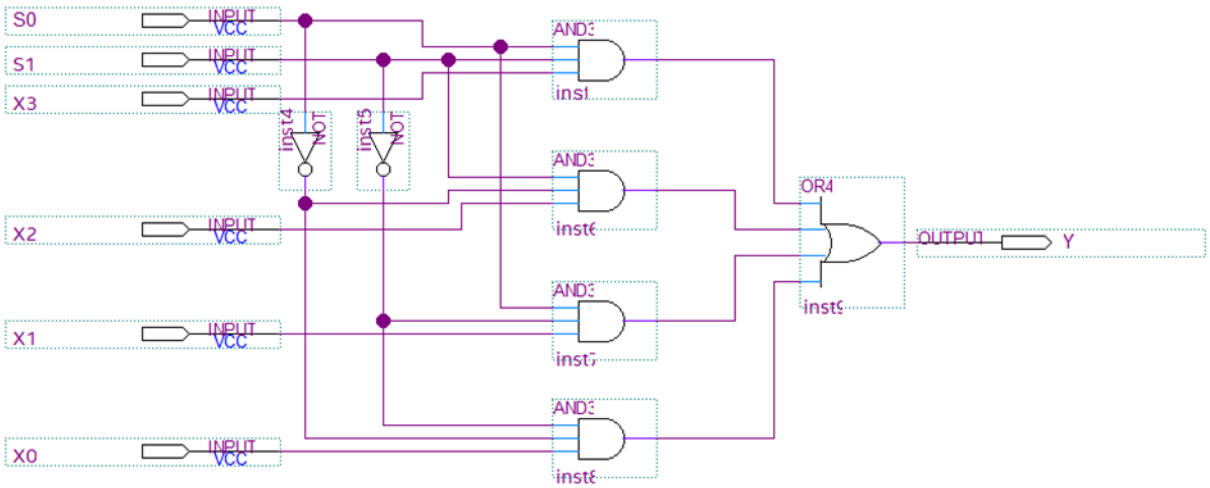

Figure 4. Schematic of 4-1 Multiplexer

Using a dataflow architecture, create the VHDL design for a 4-1 multiplexer.

Compile the design and correct any errors. The process for compiling a simulating a VHDL design is the same as for schematic entry designs.

Simulating the 4-1 Multiplexer Design

Create a vector waveform file by bringing in all four inputs, two selection inputs, and the output. Set the “Grid Size” to 100ns and the “End Time” to 800ns by going to “Edit” and “Grid Size” or “Set End Time” then entering the values (pay attention to the time units).

The vector waveform file should set up the following eight input combinations:
S1S0 = 00, X1 = 0, X2 = 0, X3 = 0, X0 = 0 and X0 = 1
S1S0 = 01, X0 = 0, X2 = 0, X3 = 0, X1 = 0 and X1 = 1
S1S0 = 10, X0 = 0, X1 = 0, X3 = 0, X2 = 0 and X2 = 1
S1S0 = 11, X0 = 0, X1 = 0, X2 = 0, X3 = 0 and X3 = 1

Perform a functional simulation and verify that the design operation is correct.

Last modified Wednesday, August 24, 2022