GEORGIA SOUTHERN UNIVERSITY

ENGR 2323 Digital Design Lab
Lab 5 State Machines

Introduction

A state machine will be designed, realized, and tested. The state machine will be realized using a solderless protoboard and discrete logic. The circuit will be tested using a powered protoboard.

Objectives

After completing this lab students should:

1. Be able to design a state machine given a state machine transition table.
2. Be able to create state diagrams corresponding to a state machine transition table.
3. Be able to realize a state machine design and create the schematic using CAD software.
4. Be able to realize and test digital circuits using discrete logic (SSI gates), a solderless protoboard, and a powered protoboard.
5. Be able to explain the operation and testing of a state machine.

Background

1. Sequential Circuit Design document.

Lab 5 Prelab

For the provided lab 5 state transition table:

- Complete the state transition table; fill in the values for the next state Q1+ and Q0+ and the output F for each row in the table.
- Create the state diagram corresponding to the state transition table. Use a drawing package such as Microsoft Visio (campus labs), Google Drawings, or draw.io to create the state diagram. Note the inputs should be named X1 and X0, the state variables Q1 and Q0, and the output F.
- Determine the MSOP next state and output expressions for the state machine.
- Create a Quartus project and enter the state machine design using the schematic editor. The schematic of the design should have a title block. For the D flip-flops for the state memory, use the Quartus DFF device rather than a 7474 device. Quartus supports virtual connections; two wires that have been named the same are equivalent to a wired connection. You may wish to have the flip-flop's clear and clock connected using virtual connections.
- Compile the design and functionally simulate the design for a vector waveform file with the inputs shown in Figure 1. Note that the inputs X1 and X0 and the state variables Q1 and Q0 have been formed into a 2-bit groups.
- Verify the design operation using the simulation results.
- Obtain datasheets for the following discrete logic chips: 74LS74. You should have the datasheets for the 74LS00, 74LS04, and 74LS20 from lab 3 and lab 4.

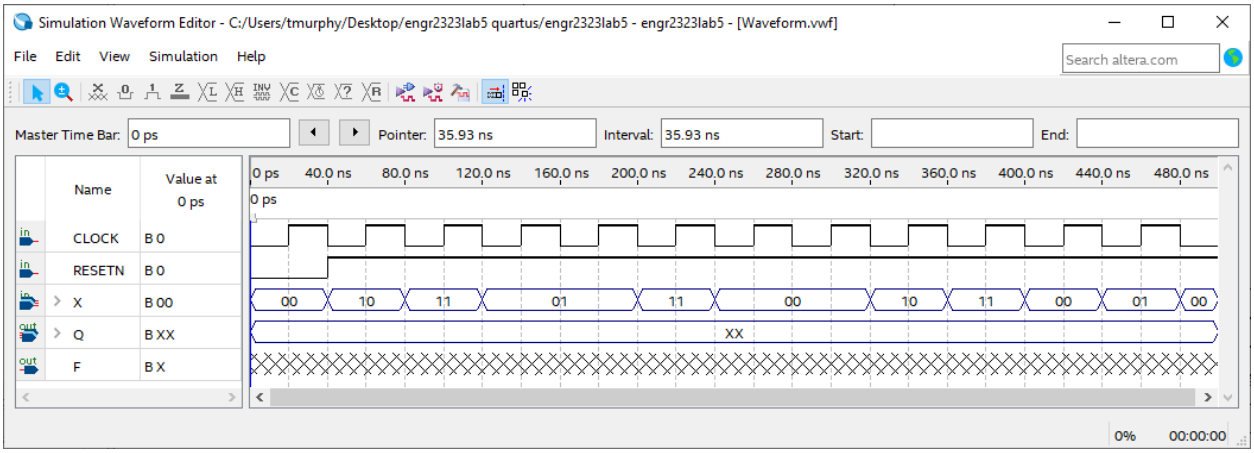

Figure 1. Functional Simulation Waveform

Lab 5

Determine the integrated circuit pin numbers for the inputs and outputs of each gate in your circuit design using the discrete logic chip datasheets.

Using the Quartus schematic editor, annotate the circuit with the device chip names (74LSXX) and annotate the inputs and outputs of each gate with the device chip pin numbers.

Using the annotated schematic, construct your circuit on a solderless protoboard. Remember that besides the gate pin connections, each integrated circuit will also need power and ground connections which are typically pins 7 and 14 on 14-pin dual inline package chips (14-pin DIP). Make sure that you have labeled or used color-coded wires for the circuit inputs and outputs. For the D flip-flops, the clear (CLR) should be connected to the circuit reset and the preset (PRE) should be deactivated. Since the preset is active low, the preset is connected to +5V to deactivate it.

You will use pushbuttons with pull up resistors for the circuit clock and reset inputs. Connect the normally open (NO) connection of the pushbutton to power through a pull up resistor and wire as shown in Figures 2a and 2b. The connection between the pushbutton and the resistor is the signal for the reset or clock.

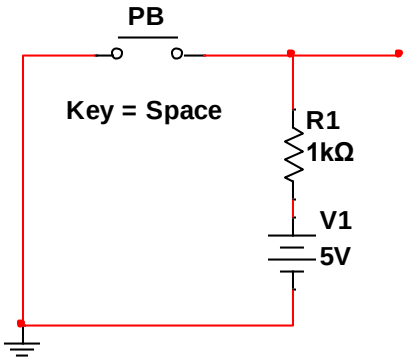

Figure 2a. Pushbutton with Pull up Resistor Schematic

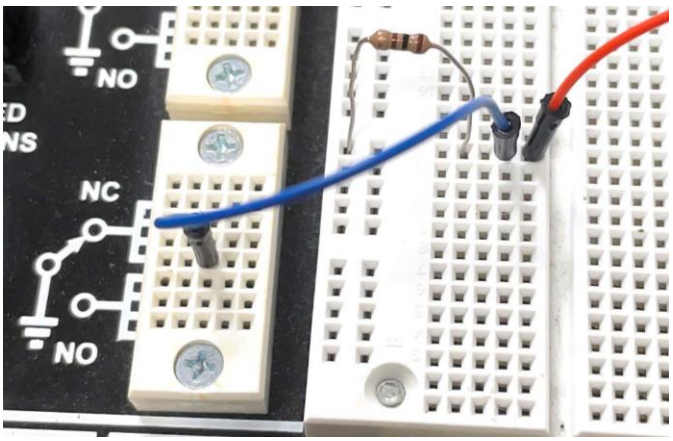

Figure 2b. PB505 Pushbutton with Pull up Resistor

Connect the powered protoboard switches 1 and 2 to the circuit inputs (switch 1 for X1 and switch 2 for X0), the top pushbutton signal to the circuit reset, and the bottom pushbutton signal to the circuit clock. Connect the circuit state Q1 Q0 to LEDs 1 and 2 and the circuit output F to LED 4.

Using the powered protoboard, verify the operation of the circuit, and demonstrate the circuit operation to the instructor. To verify the operation, test the circuit for the same input sequence that was used in the functional simulation. For each state transition, make sure to set the inputs using the switches, activate the clock by pressing the pushbutton, and verify that the next state and output are correct.

Take a picture of your constructed circuit. Make sure the lighting and contrast are good.

Lab 5 Deliverables

Lab 5 Prelab

Prelab submissions should be Microsoft Word documents and include the prelab work formatted appropriately (use the ENGR 2323 results template).

1. State transition table, state diagram, solved Karnaugh maps indicating groups and terms for next state and output expressions, and the MSOP expressions for the circuit next state and output expressions (use the ENGR 2323 function table and Karnaugh map template).

2. Quartus schematic for the state machine design.

3. Functional simulation results for the design.

Lab 5 results

Lab result submissions should be Microsoft Word documents and include the lab work formatted appropriately (use the ENGR 2323 results template).

1. State transition table, state diagram, solved Karnaugh maps indicating groups and terms for next state and output expressions, and the MSOP expressions for the circuit next state and output expressions.

2. Annotated Quartus schematic with device and pin labels for the design.

3. Functional simulation results for the design.

4. Image (appropriately cropped) of the constructed circuit.

5. Explanation of how the realized circuit operation was verified.

References
None

Last modified Thursday, September 15, 2022