ENGR 2323 Digital Design Lab
Quartus Schematic Designs

Following are the steps to create an Intel Quartus project, enter a design using schematic entry, perform device and pin assignment, compile the design, and simulate the design.

Creating a Quartus Project

Start up the Quartus Prime Lite software; the window in Figure 1a should launch.

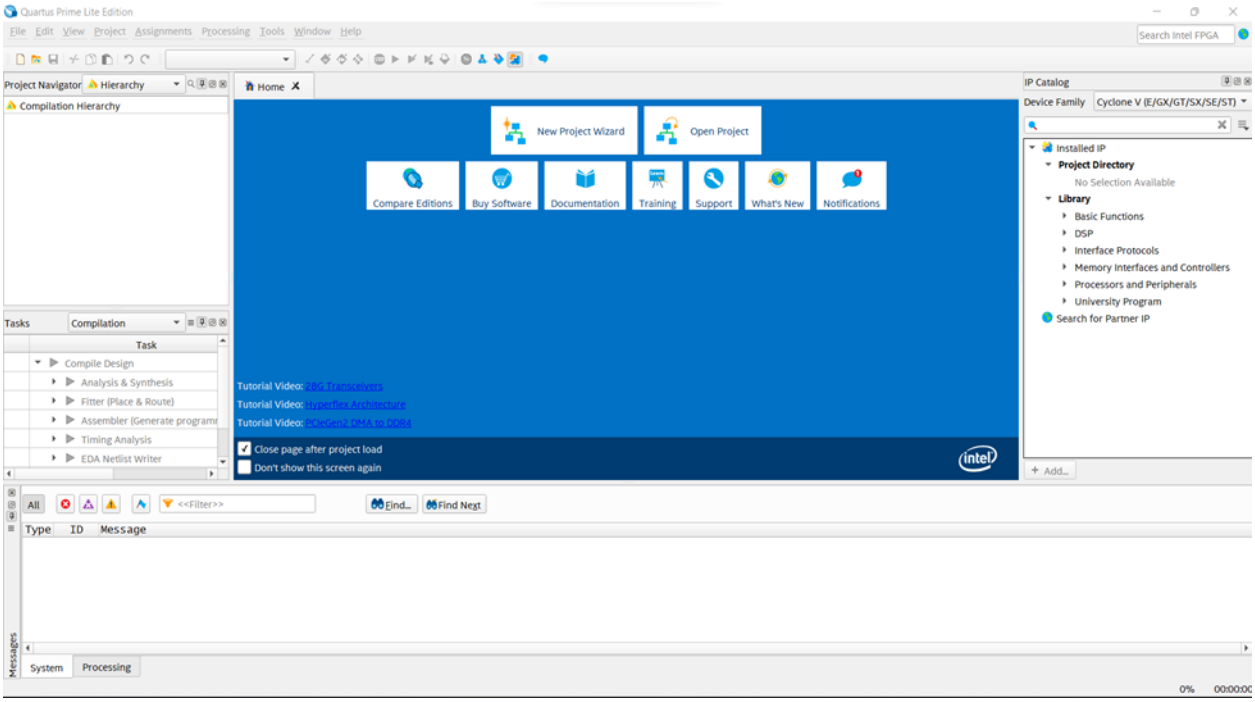

Figure 1a. Quartus Prime Lite Home Screen

Then select “New Project Wizard” from the home screen. Click “Next” to go to the directory setup, as shown in Figure 1b. Be sure to create a separate folder for each project (or labs) to avoid mixing project files. It is a good idea to create a folder named ENGR2323 on desktop and create a subfolder for each lab. Thus for lab 1, create a subfolder named Lab1. In Figure 1b, select this Lab1 folder for the “Working Directory” by clicking on “…”. You may choose any name for the project that starts with an alphabet, but something that is meaningful is a good practice. For example, for this Lab 1, you may name the project as “Lab1”. Once that is done, click “Next”.

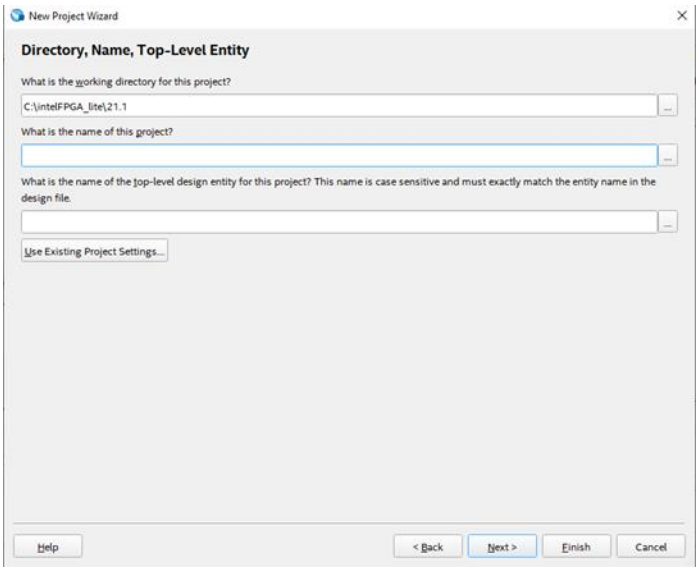

Figure 1b. Directory Setup Screen

The project type should have “Empty Project” selected (if not, then select it) then hit “Next”. There are no files to add to this project, so hit “Next” again without changing anything.

On the Family, Device, and Board Settings screen, Family should read “Cyclone V (E/GX/GT/SX/SE/ST). Next, go to the Name filter search bar on the right, and type: “5CSXFC6D6F31C6” and select it on the Available Devices list on the bottom, as shown in Figure 1c.

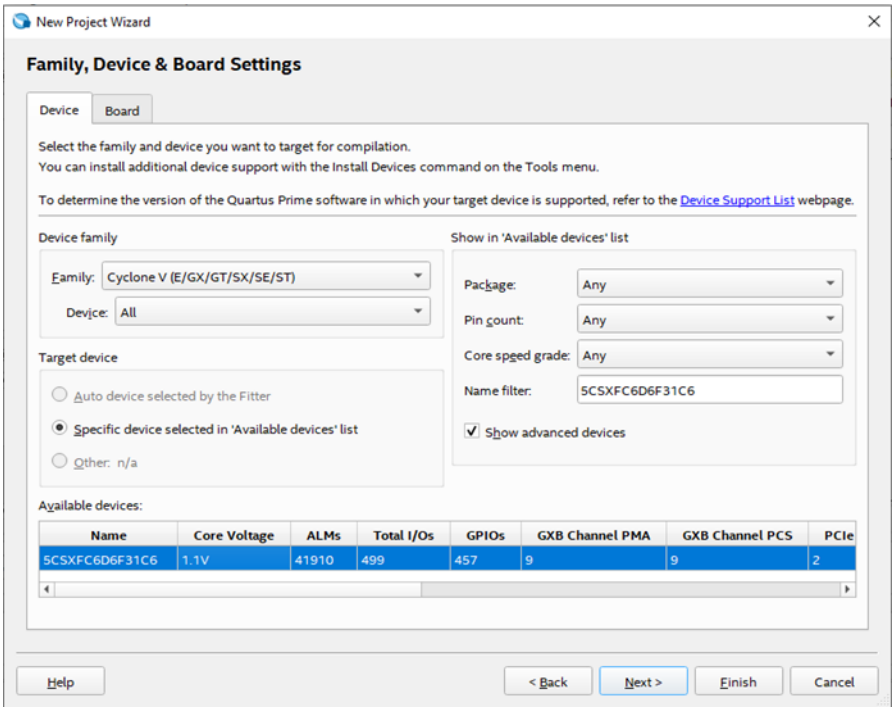

Figure 1c. Family, Device and Board Settings Screen

Now, click “Finish” and your screen should look like Figure 1d.

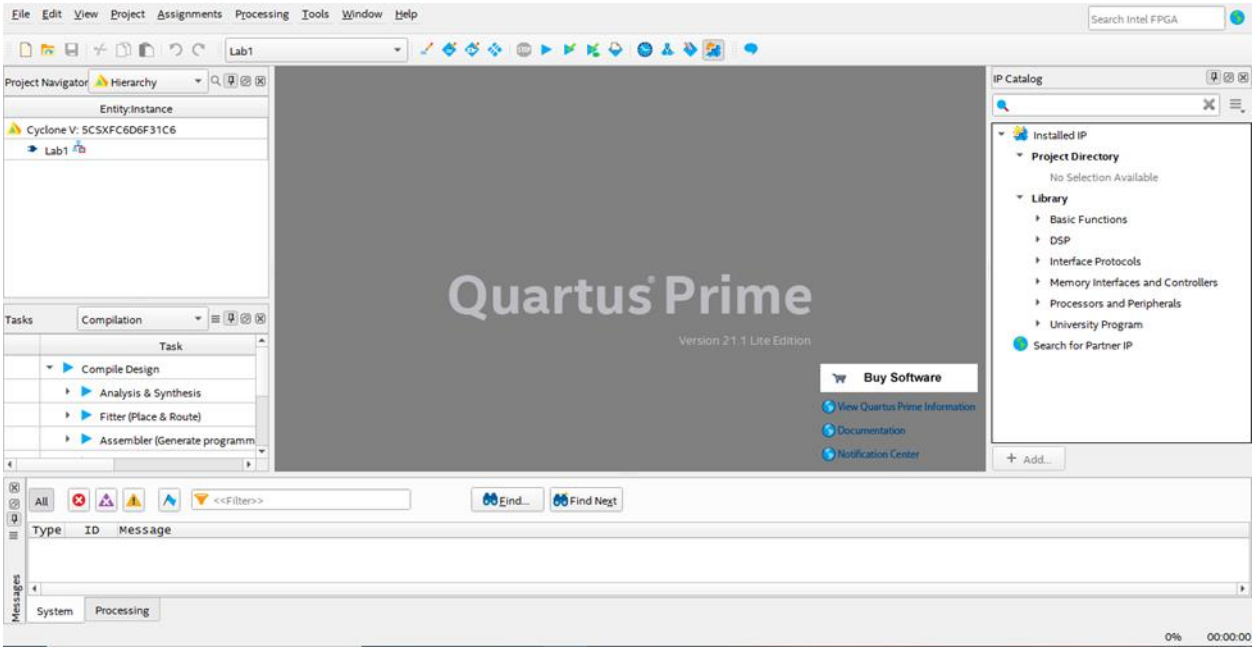

Figure 1d. Quartus Project Home Screen.

Creating a Quartus Block Diagram/Schematic

To create a block diagram/schematic, click on “File”, located on the top left toolbar, then “New”, and a pop-up menu should appear, select “Block Diagram/Schematic File”.

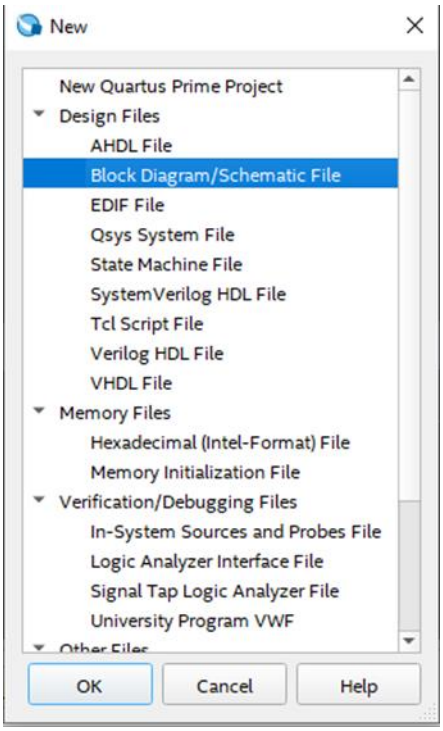

Figure 2a. New File Pop-up Menu

Now, your home screen should look like Figure 2b.

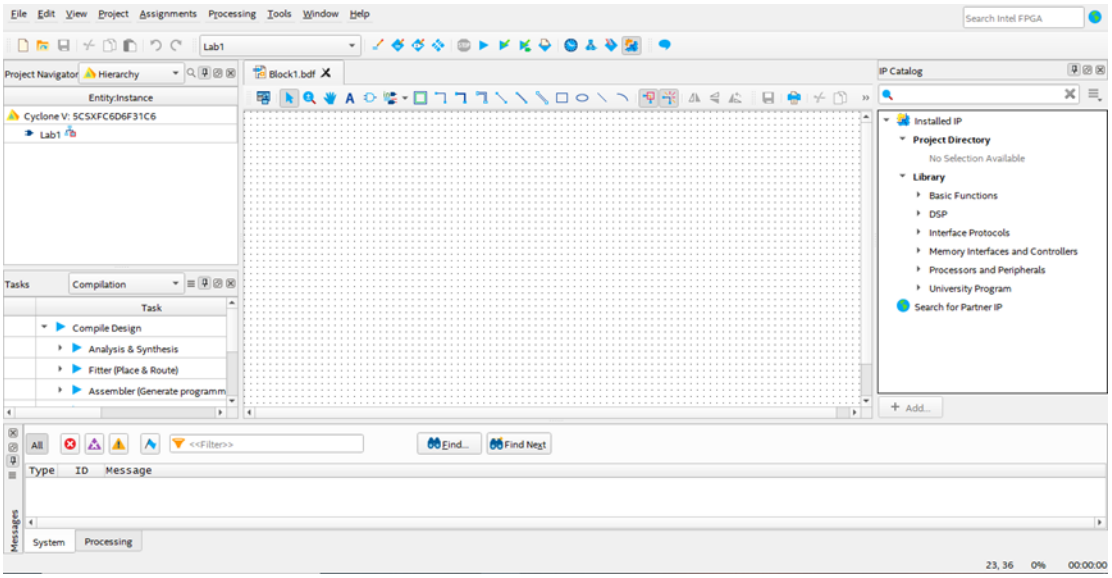

Figure 2b. Block Diagram/Schematic File Home Screen

Adding Symbols to Your Schematic Design

To add gates to your schematic, click on the “Symbol Tool” located on the new toolbar, (see Figure 2c).


Figure 2c. Block Diagram Toolbar, with "Symbol Tool" Circled.

This will bring up a pop-up screen (Figure 2d) and searching in the “Name” search bar allows you to select any gate/symbol such as AND, OR, NOT, INPUT and OUTPUT. But for gates that can have multiple inputs, a number must proceed the gate name (Figure 2d), such as AND2 or OR3.

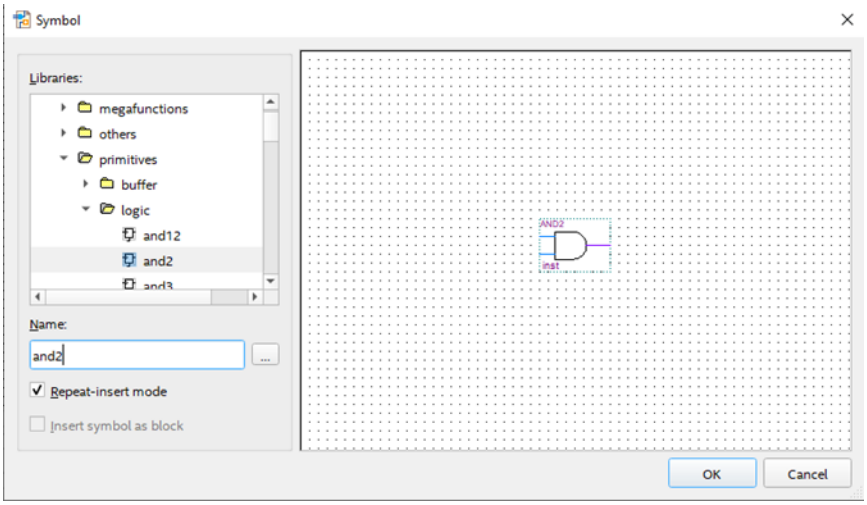

Figure 2d: Symbol Pop-up Menu and Search

After selecting the symbol to add, simply clicking on the block diagram will add it to the schematic. To deselect any symbol, click the “Selection Tool” on the tool bar (Figure 2e).

Figure 2e: Toolbar with “Selection Tool” Circled

To add inputs and outputs, you can either use the “Symbol Tool” to search for it or select the “Pin Tool” dropdown from the tool bar (Figure 2f).

Figure 2f: Toolbar with "Pin Tool" Circled

To rename inputs and outputs, double click on the pin using the selector tool, and change the Pin name.

Creating and Compiling the Multiplexer Design

Now that you know the basics of Quartus, it is time to create the 2-1 multiplexer. Your final design should look something like Figure 3a. The design should have a title block at the lower right of the design. The title block can be inserted using the Symbol Tool, typing title in the “Name” search bar, the placing the title block. Edit the fields of the title block to reflect the lab number, your name, etc. (To remove the dots, right click on a blank space on your design, go to “Show” and uncheck the “Show Guidelines” box).

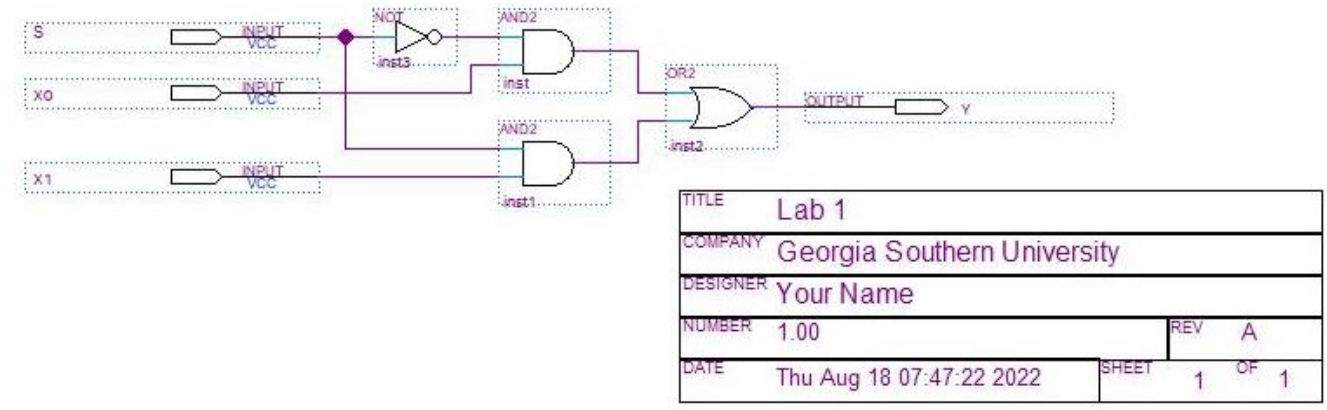

Figure 3a. 2-1 Multiplexer Design with Title Block

Now to compile your design, click on “Start Compilation” on the toolbar (Figure 3b), or press CTRL + L.

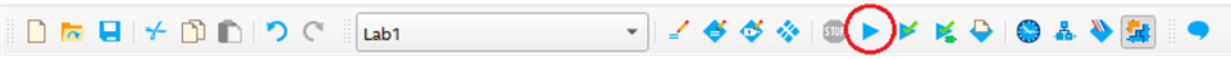

Figure 3b. Toolbar with "Compilation Tool" Circled

Compilation may take a little while, then Quartus will display all warnings and errors (if any). Warnings are generally fine, but errors will stop the compilation and must be fixed.

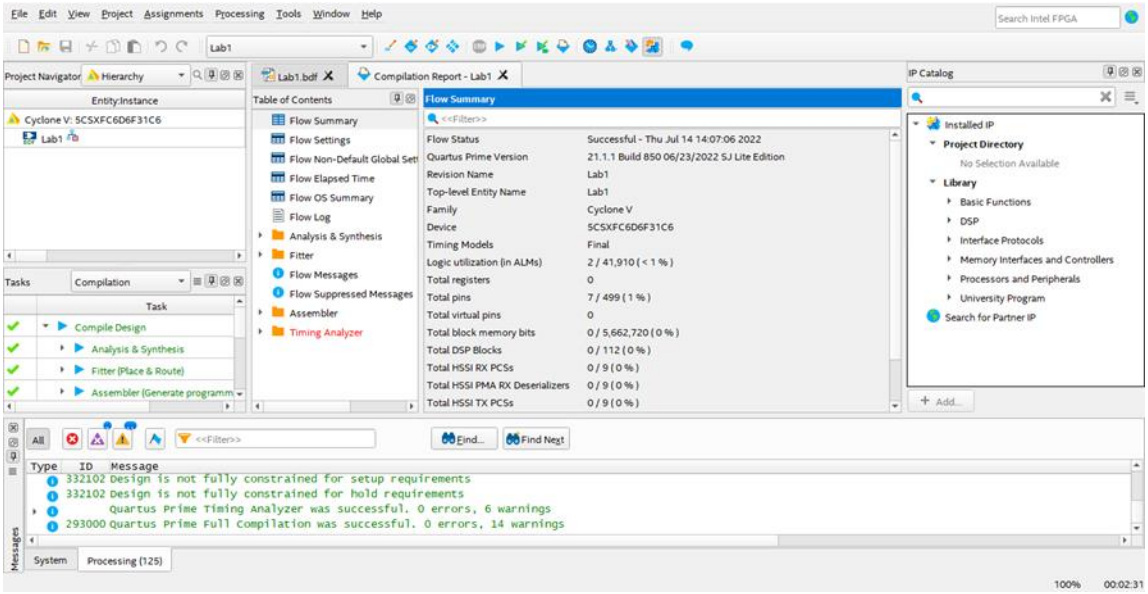

Figure 3c. A Successful Compilation Screen

Once your compilation is clear of errors, you can move to the next step.

Simulating the Design

Now that your multiplexer is created and compiled, the output can be simulated.

To simulate the circuit, a Vector Waveform file must be created. To do that, go to “File” on the top left tool bar, and select “New” (just like making the Block Schematic Diagram), and select “University Program VWF” (Figure 4a).

Now, the Simulation Waveform Editor should pop-up (Figure 4b). First, the inputs from the multiplexer need to be added. Right click under the “Name” column on the left, and select “Insert Node or Bus”, another window should appear, select “Node Finder” on the right and other window will appear. Click “List” on this new window to list the inputs from the schematic file. Press the “>>” button to transfer them to the VWF file. Then click “OK” to exit the Node Finder. (Figures 4c -4e).

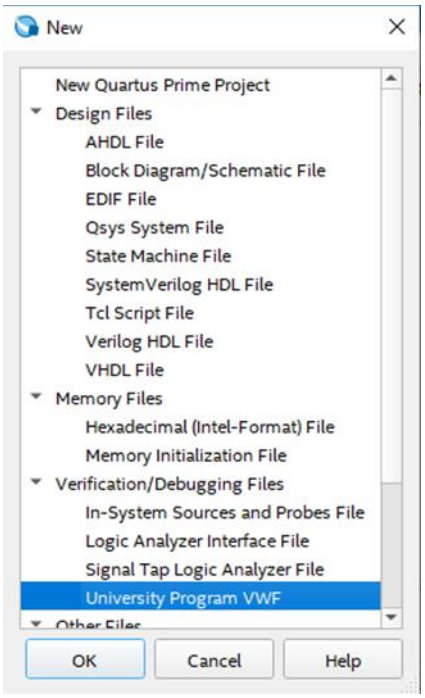

Figure 4a. VWF File Selection

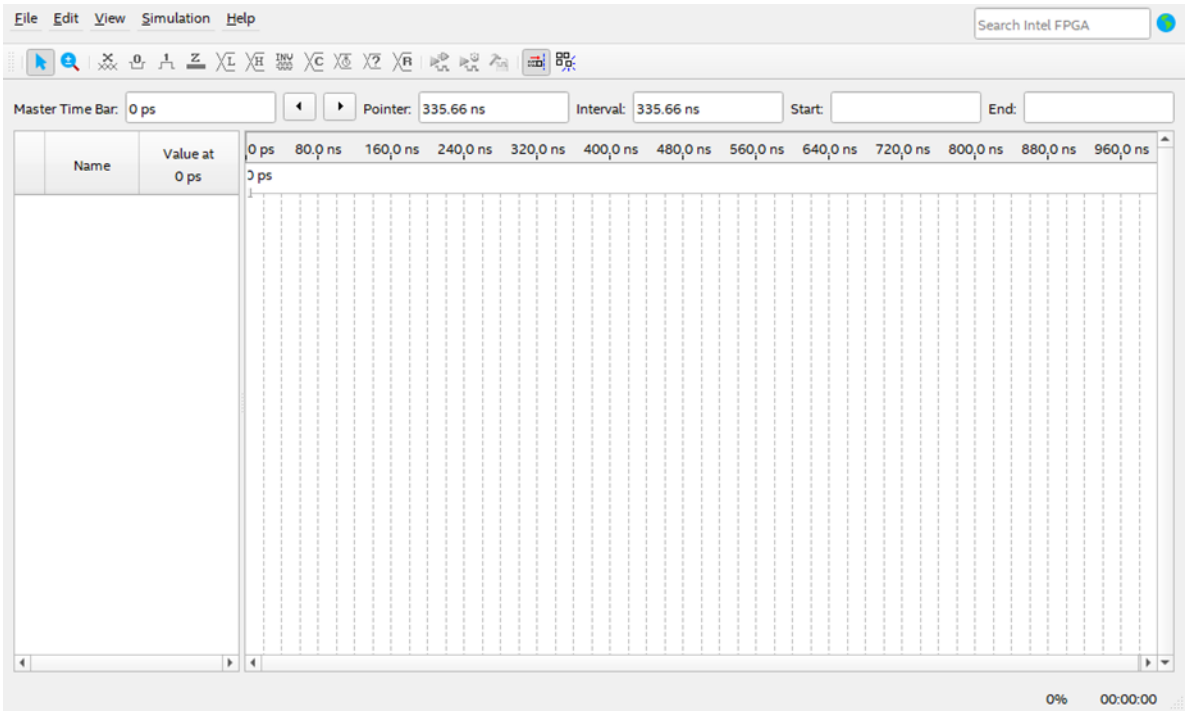

Figure 4b. Simulation Waveform Editor Window

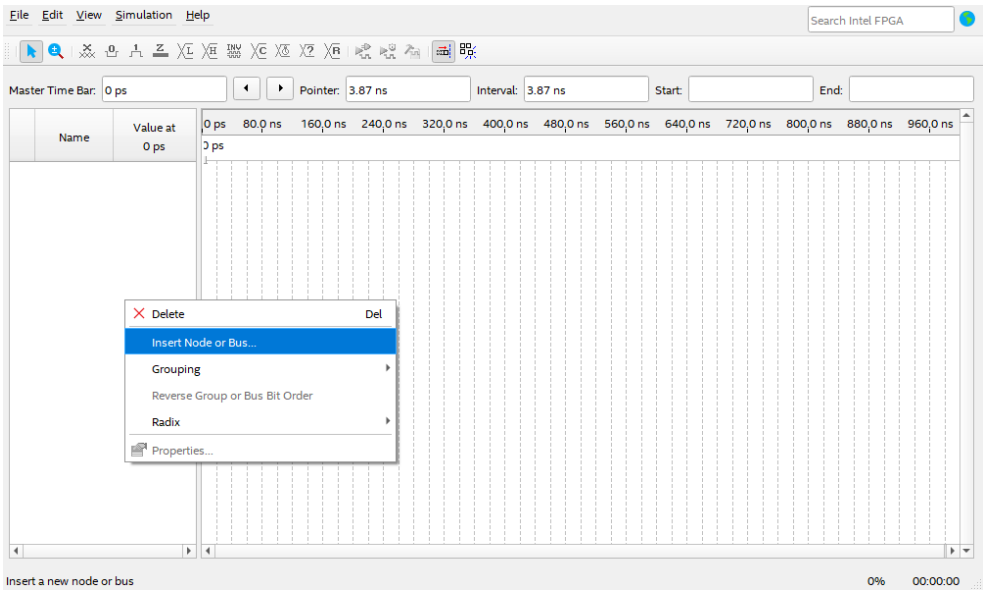

Figure 4c. Inserting Node or Bus

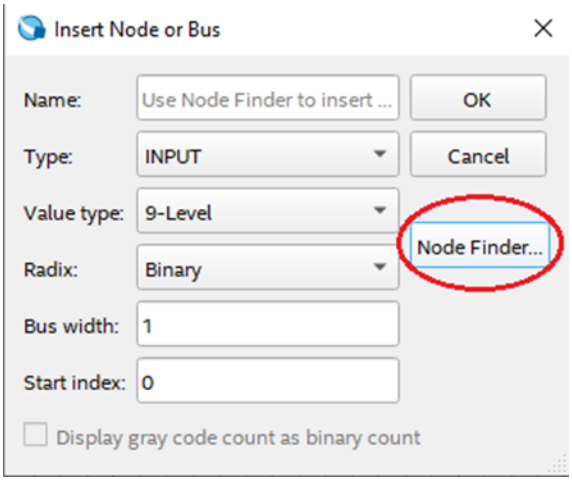

Figure 4d. Insert Node or Bus Screen

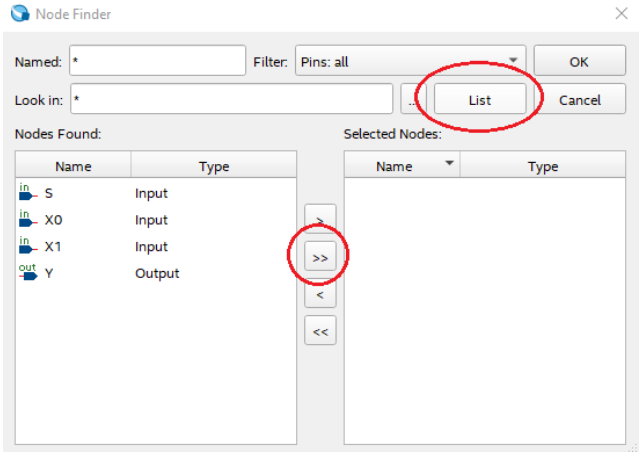

Figure 4e: Node Finder Screen

Your simulation screen should look something like Figure 4f.

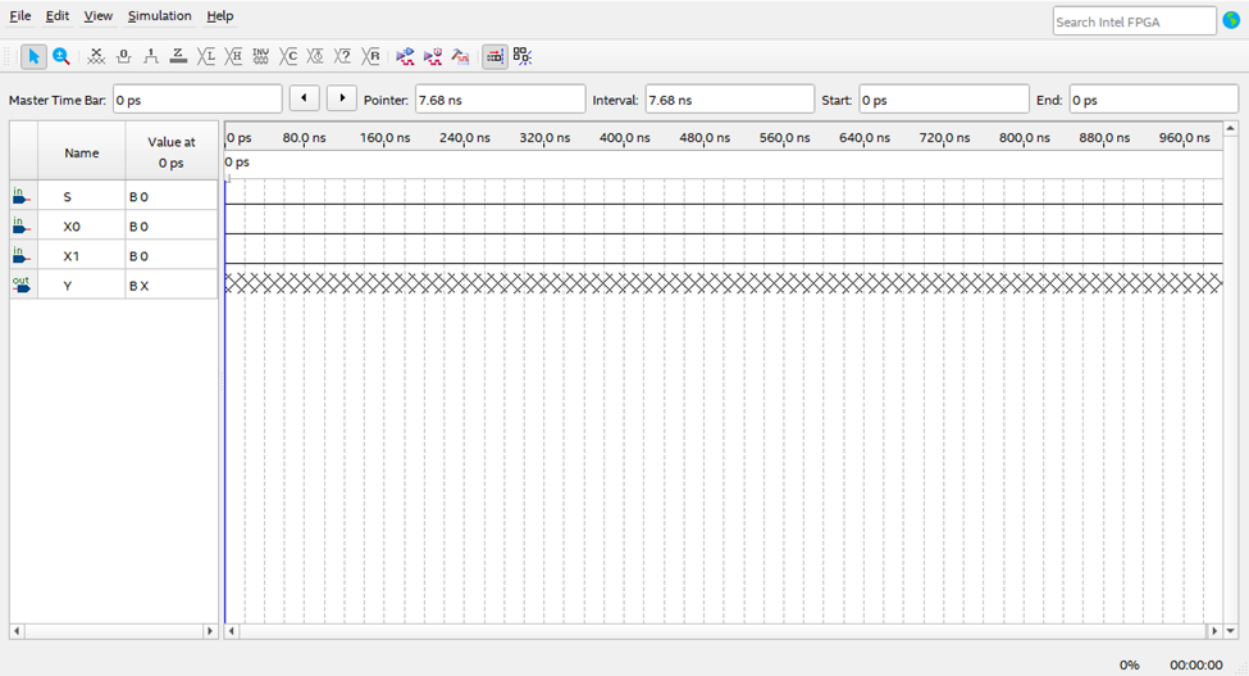

Figure 4f. Simulation Screen with Nodes

Now, edit the Grid Size to 50ns and the End Time to 800ns by going to “Edit” and “Grid Size” or “Set End Time” then inputting the values (Pay attention to units!).

To add values to the inputs, double click then right click on the waveform interval, then go to “Value” and “Count Value” and change the interval (Figures 4g and 4h).

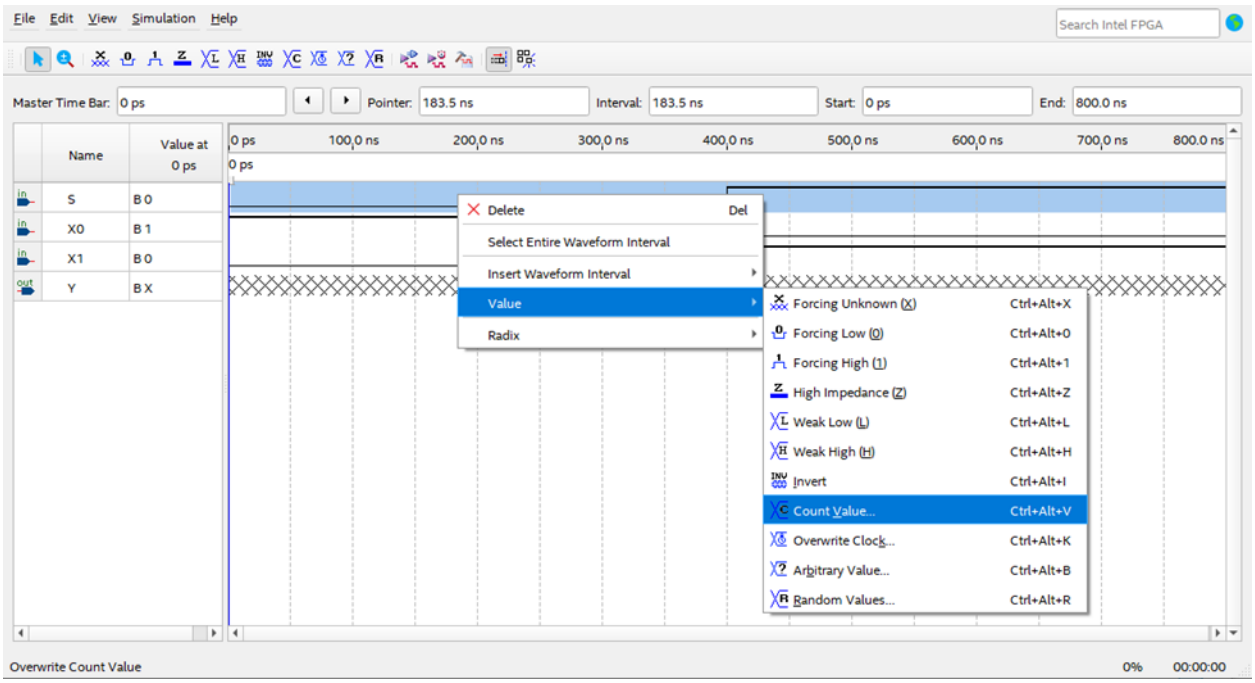

Figure 4g. Selecting the “Count Value” Option.

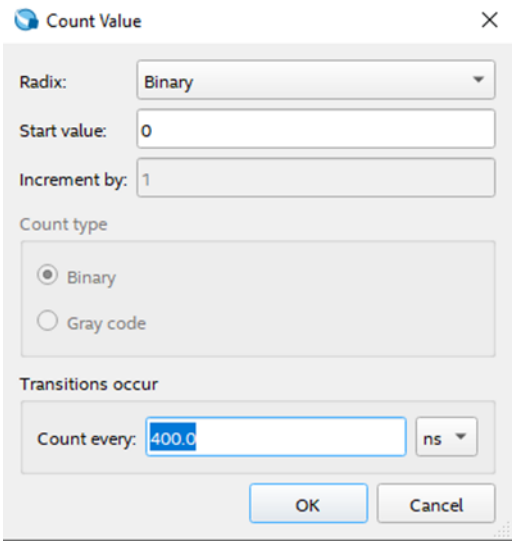

Figure 4h. Changing the Count Value

The Input values should be the following:
S = Count value of 400, starting from 0.
X0 = Count value of 200, starting from 0 for first half of time (0 – 400 ns) and X0 = 0 for second half of time (400 – 800ns).
X1 = 0 for first half of time (0 – 400 ns) and X1 = count value of 200, starting from 0 for second half of time (400 – 800ns).
Y is an output, so it does not need to be edited.

Your completed VWF file should look like Figure 4i.

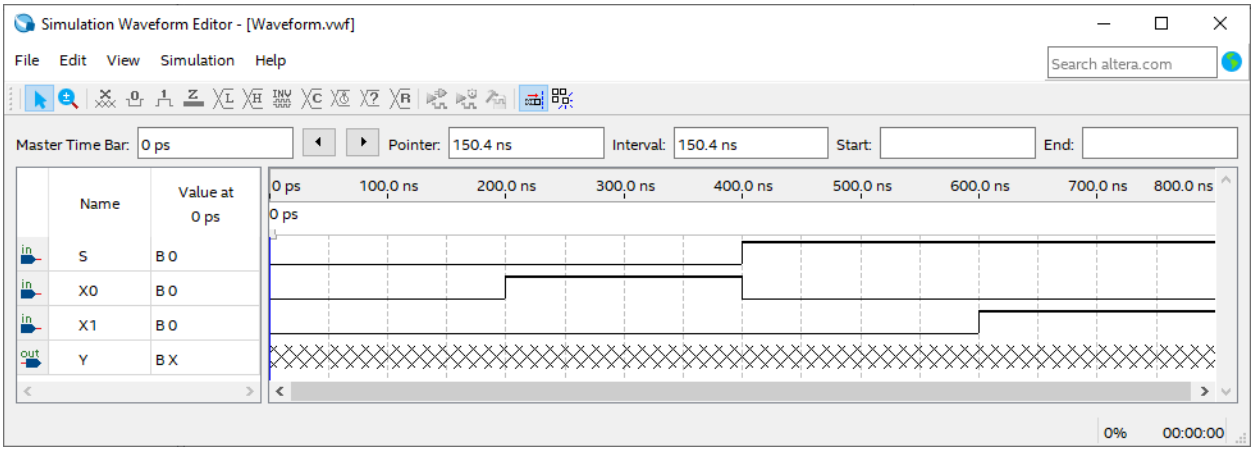

Figure 4i. Completed VWF File

Now you are ready simulate. Select the “Run Functional Simulation” button from the toolbar. It will ask you to save the VWF file, changing the name can complicate things, so do not change it.


Figure 4j. Functional Simulation Button

For the Timing Simulation, press the “Run Timing Simulation” button from the toolbar, right next to the Functional Timing button (Figure 4k).


Figure 4k. Timing Simulation Button

For both simulation options, A window should pop-up to run the code, and then a read only output file should be created which should look like Figure 4l.

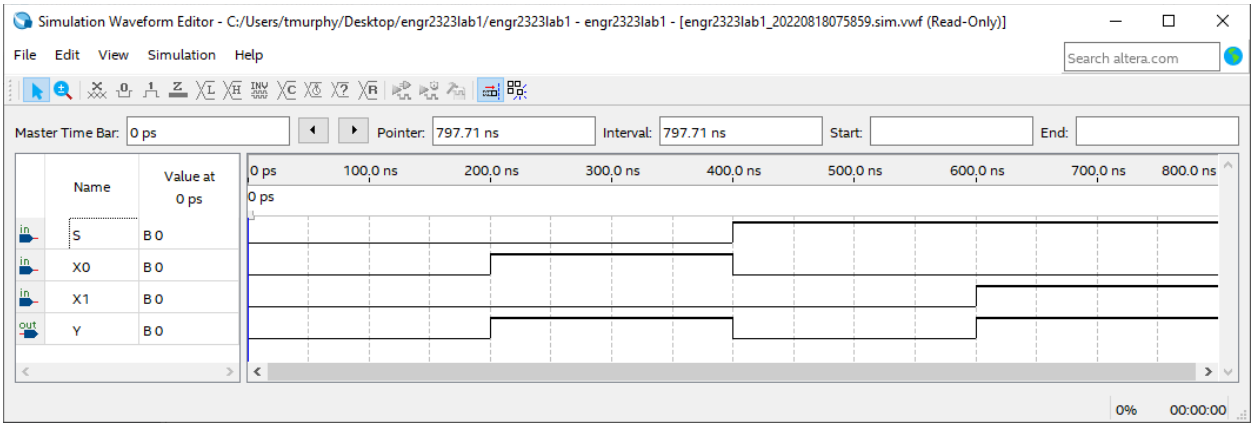

Figure 4l. Read-only Output File

Last modified Thursday, August 18, 2022