ENGR 2323 Digital Design Lab
Lab 1: Introduction to Computer Aided Digital Design

Introduction

A 2-1 multiplexer will be designed and simulated using Intel Quartus Prime Lite CAD software. The design will be implemented and tested using a DE10-standard FPLD development board.

Objectives

After completing this lab students should:

1. Be able to create schematic designs using Intel Quartus CAD software.
2. Be able to perform functional and timing simulations of designs using Intel Quartus CAD software.
3. Be able to implement designs by programming FPGAs.
4. Be able to verify the operation of a design.

Background

1. Digital Logic Technologies document (Readings)
2. Installing Intel Quartus Prime Lite document (Readings)
3. Quartus Schematic Design document (Readings)
4. Programming DE10 Board document (Readings)

Lab 1 Prelab

Follow the steps in the Quartus Schematic Design document (Readings) and

- Create a Quartus project and enter the design for a 2-1 multiplexer using the schematic editor. The design should target the Cyclone V chip on the DE10-standard board. The schematic of the design should have a title block.
- Compile the design and make sure there are no errors (warnings are generally ok).
- Assign pins for the inputs and outputs of the design
- Recompile the design and make sure there are no errors.
- Perform a functional simulation of the design.
- Perform a timing simulation of the design.

Bring the entire Quartus design project folder and your prelab work to lab.

Lab 1

Copy your project folder from the prelab to the desktop of the lab computer.

Launch Quartus by double clicking on the project file in the folder.

Open the design schematic if it did not open automatically.

Recompile the design and make sure there are no errors and the project device and pin assignments are correct for the DE10-standard board.

Follow the steps in the Programming the DE10-standard board document (Readings) and program the FPLD on the development board.

Verify the operation of the design on the board, i.e. go through all of the input combinations using the slides switches and verify the output on the LED is correct for each input combination.

Lab 1 Deliverables
Lab 1 Prelab
Prelab submissions should be Microsoft Word documents and include the prelab work formatted appropriately (use the ENGR 2323 results template).

1. Quartus schematic of 2-1 multiplexer schematic with pin assignments and title block.

2. Functional simulation results.

3. Timing simulation results.

Lab 1 results
Lab result submissions should be Microsoft Word documents and include the lab work formatted appropriately (use the ENGR 2323 results template).

1. Quartus schematic of 2-1 multiplexer schematic with pin assignments and title block.

2. Functional simulation results.

3. Timing simulation results.

4. Images of the DE10-standard board showing the output Y for two of the test combinations: S = 0 and x0 = 0 and S = 0 and x0 = 1 (two images one for each combination). Make sure the image shows the input switch positions and the LED for the output.

5. Brief explanation of how the design operation was verified.

References
None

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