Lab 1

ENGR 2323

Digital Design Lab

Date:

Class Outline

- Digital design process.
- Discrete logic.
- Custom Integrated Circuits.
- PLD, FPGA
- Intel Quartus Designs.
- Lab 1 deliverables.

Objectives

- Be able to create schematic designs using Intel Quartus CAD software.
- Be able to perform functional and timing simulations of designs using Quartus CAD software.
- Be able to implement and test designs using FPLD development boards.

Important Terms/Concepts

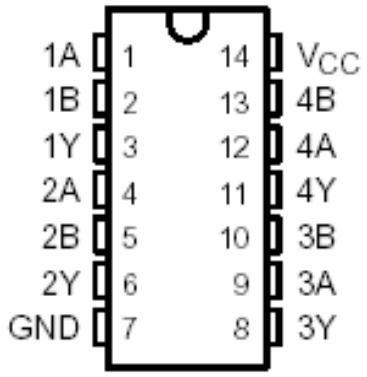
- Computer aided design software is needed for designing and verifying the operation of complex digital designs. CAD software typically supports schematic and hardware description language (HDL) designs and function and timing simulations.
- Important terms/concepts include:
  - Discrete logic
  - PLD, FPGA
  - ASIC, ASSP
  - CAD
  - Schematic entry, Functional simulation

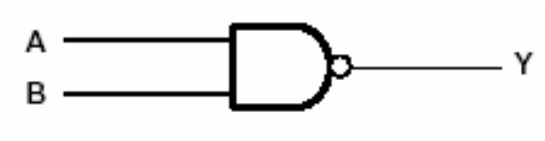
Digital Circuit Design

- Digital circuits are typically designed using CAD software.
  - The designs are entered using schematic entry, hardware description language, or a combination of both.
  - The design is functionally simulated to ensure the logical operation is correct and then simulated with timing constraints.
- The design can be implemented using: discrete logic, programmable logic, and full custom integrated circuits (ASIC/ASSP).
- If the design is to be implemented using a FPGA, the CAD software is used to partition and map the design to the function blocks of the programmable device.

Discrete Logic

- Discrete logic is traditional off the shelf integrated circuits. They are typically SSI (2-8 gates per chip) or MSI devices (up to a few hundred gates per chip).
- The devices have a fixed operation (hardwired inputs and outputs) defined by the manufacturer. For example, a 74HCT00 is a quad 2-input NAND gate.





Custom Integrated Circuits

- Application specific integrated circuits (ASIC) are a custom integrated circuit for a particular application. The design is sent to a fabrication plant for implementation. Design modification is difficult late in the design process and testing can be more difficult. ASICs have a very high non-recurring engineering (NRE) cost and are only cost effective in high volumes.
- Application–specific standard product chips are in between standard logic (7400, 4000 series) and ASICs. They are comparable to ASICs in performance but are not full custom so are often lower cost.

Programmable Logic Devices

- Programmable Logic Devices (PLDs) are integrated circuits where the internal operation is defined (programmed) by the user.
- PLDs contain a matrix of logic cells along with input and outputs that can be interconnected. The logic cells typically are: logic gate structures (AND-OR), multiplexers, or look up tables (memory).
- Modern FPGAs contain upwards of 40 billion transistors (10 million logic elements).
- Intel Cyclone V 5CSXFC6 is a system on a chip FPGA. It has 110k logic elements, a dual core Arm Cortex A9 processor, 112 DSP blocks, and around 6.2Mb of embedded memory. It has 228 input/output pins.
- For prototyping and designs with lower production, FPGAs are often cheaper and more practical.

Intel Quartus Designs

- Designs will be created using Intel Quartus CAD software.
  - Make sure you are using Intel Quartus Prime Lite v18.1.
  - Lab 1 will involve a schematic entry design.
  - Make sure project name and top-level design file are the same.
  - Project path to the project files cannot have spaces in the name. Work from a folder on the desk.
  - Make sure design has title block.
  - Make sure to assign the correct device for your project. Designs are compiled for targeted FPGA. The DE10-standard boards have a Cyclone V 5CSXFC6D6F31C6 FPLD.
  - Make sure pin assignments are correct and that unused pins (unused FPGA pins) are set as input tri-stated.
  - Make sure to compile the design, otherwise will not be able to simulate design or program FPGA with design.

Verifying Design Operation

- Make sure you know what the design you are simulating or testing on the development board is supposed to do, i.e. be able to compare the waveforms or behavior to logic expressions and/or function table of the schematic.
- If the functional simulation is correct, then the design should be logically correct. If your design does not work on the development board, check that the device and pin assignments are correct.

Lab 1 Deliverables

- Lab 1 Prelab
  - Quartus schematic of 2-1 multiplexer schematic with pin assignments and title block.
  - Functional simulation results.
  - Timing simulation results.
- Lab 1 Work
  - Program the DE10-standard FPLD with your design and verify the design operation.
- Lab 1 Results
  - Quartus schematic of 2-1 multiplexer schematic with pin assignments and title block.
  - Functional simulation results.
  - Timing simulation results.
  - Images of the DE10-standard board showing the output for each value of the selection input.
  - Brief explanation of how the design operation was verified.