ENGR 2323 Digital Design Lab
Combinational Circuit Design

Boolean Expressions and Standard Forms

Boolean expressions (logic expressions) can be used to describe the operation of a digital circuit. A sum of products (SOP) expression is one or more AND terms ORed together, for example $F = \overline{A} \cdot B + B \cdot C + A \cdot \overline{B}$.

There are usually many equivalent ways to represent a particular expression. A standard or canonical sum of products (CSOP) is a SOP where every AND term includes every independent variable (each term is a minterm), for example $F = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot C + A \cdot B \cdot \overline{C}$.

Boolean Expressions can be simplified using Boolean Algebra manipulation (not always straight forward).

$$F = \overline{A} \cdot B + B \cdot C + \overline{A} \cdot \overline{B} = \left(\overline{A} \cdot B + \overline{A} \cdot \overline{B}\right) + B \cdot C$$

$$F = \overline{A} \cdot \left(B + \overline{B}\right) + B \cdot C = \overline{A} + B \cdot C$$

For five or fewer variables, Karnaugh maps can be used for simplification. Karnaugh maps are set up such that only one independent variable value changes between adjacent minterms. To simplify a Boolean expression using a Karnaugh map (find a minimum sum of products, MSOP): first put the minterms on the Karnaugh map, next identify all the prime implicants for the map, form product terms for each essential prime implicant and enough non-essential prime implicants so that all 1s in the map are included, the MSOP is obtained by ORing the product terms formed together.

The function table of Figure 1a describes the operation of a circuit with three inputs and one output.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Figure 1a. Function Table

The CSOP corresponding to the function table is $F = \sum_{ABC}(0,1,4,6,7)$. To determine the MSOP using a Karnaugh map (Figure 1b), adjacent ones are grouped (Figure 1c) and simplified product (AND) terms are written for each group. The product terms are then ORed together.

A/BC	00	01	11	10
0	1	1	0	0
1	1	0	1	1

Figure 1b. Karnaugh Map

A/BC	00	01	11	10
0	1	1	0	0
1	1	0	1	1

Figure 1c. Karnaugh Map with Groups Identified

The Karnaugh map of Figure 1c has three groups, the two horizontal groups (in red) correspond to the essential prime implicants and the one vertical group (in green) is a non-essential prime implicant.

The essential prime implicants consist of minterms 0 and 1 (m0, m1) and minterms 6 and 7. The non-essential prime implicant consists of minterms 0 and 4.
The terms for the three groups are
Group m0, m1: $\overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C = \overline{A} \cdot \overline{B}$
Group m6, m7: $A \cdot B \cdot \overline{C} + A \cdot B \cdot C = A \cdot B$
Group m0, m4: $\overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} = \overline{B} \cdot \overline{C}$
And the MSOP expressions corresponding to th truth table is
$F = \overline{A} \cdot \overline{B} + A \cdot B + \overline{B} \cdot \overline{C}$

There is a second non-essential prime implicant that consists of minterms 6 and 7 that is not needed for the MSOP as all the 1s are grouped without it. It could be used in place of the group of minterms 0 and 4.

Combinational Circuit Design
Sum of products (SOP) expressions require one level of AND gates followed by a OR gate for each output. By simplifying the expression to the MSOP form, the number of gates and number of inputs to the gates may be reduced. NAND – bOR (NAND – NAND) realizations are often used rather than AND-OR realizations since the transistor count is lower and the resulting circuit is usually faster for devices in the same logic family.

The two level AND-OR realization for $F = \overline{A} \cdot \overline{B} + A \cdot B + \overline{B} \cdot \overline{C}$ is shown in Figure 2a. The corresponding mixed logic NAND - bOR realization for $F = \overline{A} \cdot \overline{B} + A \cdot B + \overline{B} \cdot \overline{C}$ is shown in Figure 2b.

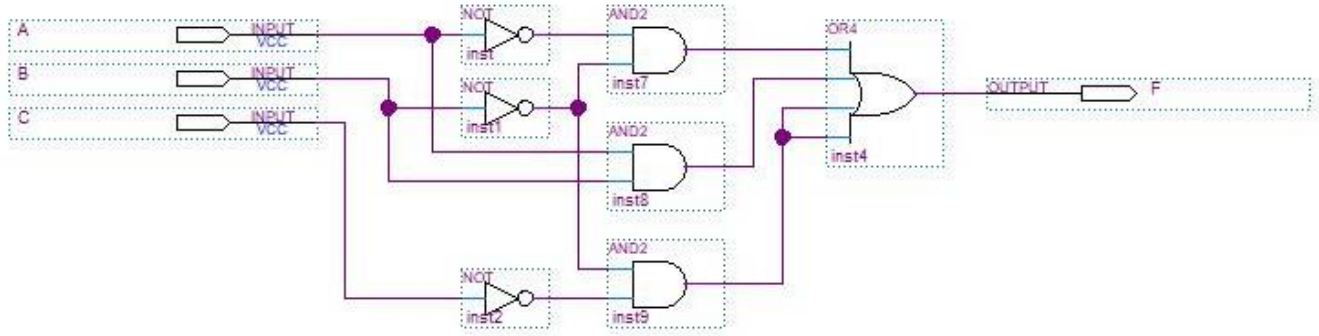

Figure 2a. AND-OR Realization of a MSOP

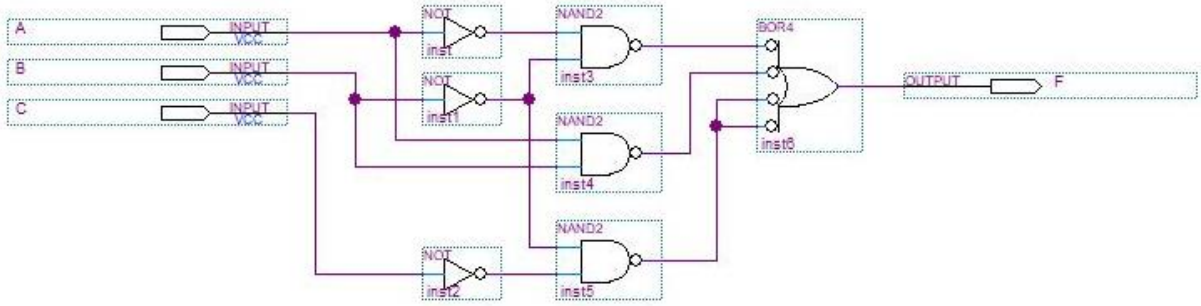

Figure 2b. NAND-bOR (NAND-NAND) Realization of a MSOP

Note that in the circuits of Figures 2a and 2b a four input OR gate is used instead of a three input gate. The number of inputs required for a gate is not always commercially available. Although three input OR and three input NAND gates are available, these circuits illustrate how to use a gate with more inputs to realize a term requiring fewer inputs; the extra gate inputs are tied to one of the other inputs.

Annotated Schematics for Realizing Designs using Discrete Logic

Digital circuit prototypes are commonly built using solderless protoboards and dual inline package integrated circuits. Dual inline package (DIP) integrated circuits have two rows of pins with a plastic or ceramic body and can be used with solderless and soldered protoboards.

Before constructing the circuit, the specific device and pin connections between devices must be determined. Manufacturer data sheets provide the pin information for the integrated circuits and the pins depend on the package type. Schematics can be annotated using the Quartus text tool. The gates in the design may need to be spread out so that the labels are clear and readable in the schematic.

Figure 3 shows an annotated version of the circuit of Figure 2b. The discrete logic integrated circuits for the gates are: 74LS04 (hex inverter) for the NOT gates, 74LS00 (quadruple 2-Input positive-NAND gates) for the 2-input NAND gates, and 74LS20 (dual 4-input positive NAND gates) for the 4-input NAND (bOR) gate.

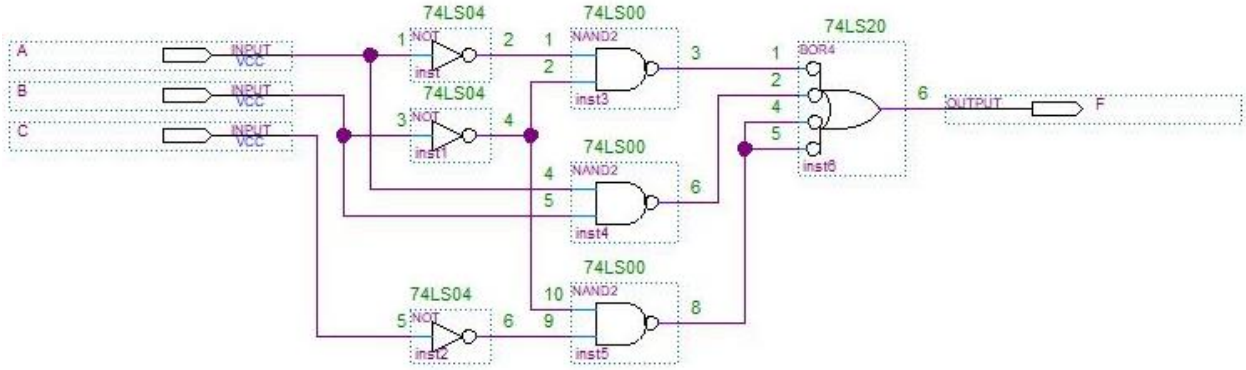

Figure 3. NAND-bOR (NAND-NAND) Realization of a MSOP

The top NOT gate is labeled with the integrated circuit (74LS04) at the gate input and output are labeled with the pin numbers for the first NOT gate on the integrated circuit. The second NOT gate is pins 3 and 4, and the third NOT gate pins 5 and 6. A single 7404 chip provides all the needed NOT gates with three spares. Three of the four 2-input NAND gates of the 7400 are used and one of the two 4-input NAND gates of the 7420 is used in the design.

The annotated schematic does not show the power and ground connections for the integrated circuits. For 14-pin DIPs, ground is typically pin 7 (lower right pin) and power is pin 14 (upper left pin). To test the constructed circuit, the circuit inputs would be connected to switches or push buttons and the circuit outputs to LEDs.

References

None

Last modified Tuesday, July 12, 2022