ENGR 2323 Digital Design Lab
Lab 6 State Machine Design and Testing

Introduction

A state machine will be designed, realized, and tested. The state machine will be described using VHDL and implemented and tested using a DE10-standard FPLD development board and a mixed signal oscilloscope/logic analyzer.

Objectives

After completing this lab students should:

1. Be able to design sequential circuits using a hardware description language such as VHDL.
2. Be able to verify sequential circuit design operation using simulations and testing on a FPGA development board.
3. Be able to verify sequential circuit design operation using a mixed signal oscilloscope/logic analyzer.

Background

1. State Machine Design using VHDL document (add link)
2. Logic analyzer document (add link)
3. Logic analyzer video (add link)

Lab 6 Prelab

For the state transition table used for Lab 5:

- Create a Quartus project and VHDL state machine design using a behavioral architecture. The behavior architecture can be design using either the state transition table or state diagram from Lab 5. The entity for the design should match the entity of Figure 1.
- Compile the design and simulate the design for a vector waveform file with the inputs shown in Figure 2. This is the same set of simulation inputs as was used in Lab 5.
- Verify the design operation using the simulation results.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY state_machine IS
PORT(CLOCK : STD_LOGIC;
     RESETN : STD_LOGIC;
     X : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
     Q : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
     F : OUT STD_LOGIC);
END state_machine;
```

Figure 1. Entity for VHDL State Machine Design

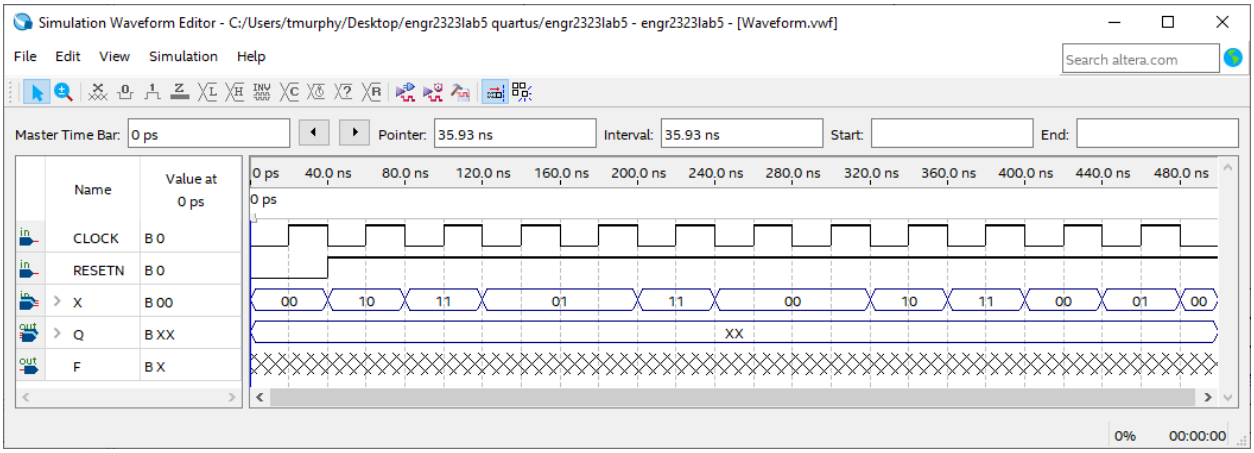

Figure 2. Functional Simulation Waveform

Lab 6

Open your Quartus project from the prelab. Open the VHDL design if it did not open automatically.

Recompile the design and make sure there are no errors and the project device assignment is correct for the DE10-Standard board.

Using the pin planner, assign pins for the inputs and outputs of the design according to Table 1. The state variables are not typically an output of a sequential circuit but having access to the state is useful when testing and debugging a sequential circuit design. The pin assignments corresponding to the DE10-Standard devices can be found in the DE10-Standard Pin Assignments document. The Key inputs are the DE10-Standard pushbuttons. Make sure to also set the FPGA unused pins as inputs tri-stated.

Input	**DE10-Standard Device**
CLOCK	Key[0]
RESETN	Key[3]
X1	SW[1]
X0	SW[0]
Q1	LEDR[2]
Q0	LEDR[1]
F	LEDR[0]

Table 1. Input and Output Assignments for State Machine

Recompile the design and make sure there are no errors.

Program the DE10-Standard board FPGA with your design. Refer to Programming DE10-Standard Board document.

Verify the operation of the state machine and demonstrate the circuit operation to the instructor. To verify the operation, test the circuit for the same input sequence that was used in the simulation.

Add steps for verifying operation using logic analyzer

Lab 6 Deliverables
Lab 6 Prelab
Prelab submissions should be Microsoft Word documents and include the prelab work formatted appropriately (use the ENGR 2323 results template).

1. State transition table and state diagram for the state machine. These should be the same as developed for Lab 5.

2. Behavioral VHDL design for state machine. This should be formatted using the Program code block style.

3. Functional simulation results for the design.

Lab 6 results
Lab result submissions should be Microsoft Word documents and include the lab work formatted appropriately (use the ENGR 2323 results template).

1. State transition table and state diagram for the state machine.

2. Behavioral VHDL design for state machine.

3. Functional simulation results for the design.

4. Oscilloscope screen capture showing the state machine operation.

5. Explanation of how the design operation was verified on the DE10-Standard board and using the logic analyzer.

References
None

Last modified Tuesday, September 20, 2022