Lab 7

ENGR 2323

Digital Design Lab

Class Outline

- Design of Mod 10 up/down counter
- Clock/frequency division
- Programming seven segment LEDs in DE -10 board
- Lab 7 deliverables.

Objectives

1. Be able to fortify their understanding of designing a state machine through state diagram and state table
2. Be able to implement a practical FSM design through VHDL
3. Be able to understand about clock frequency and clock division for practical implementation of certain digital circuits.
4. Be able to understand the use of seven segments in DE-10 board

Important Terms/Concepts

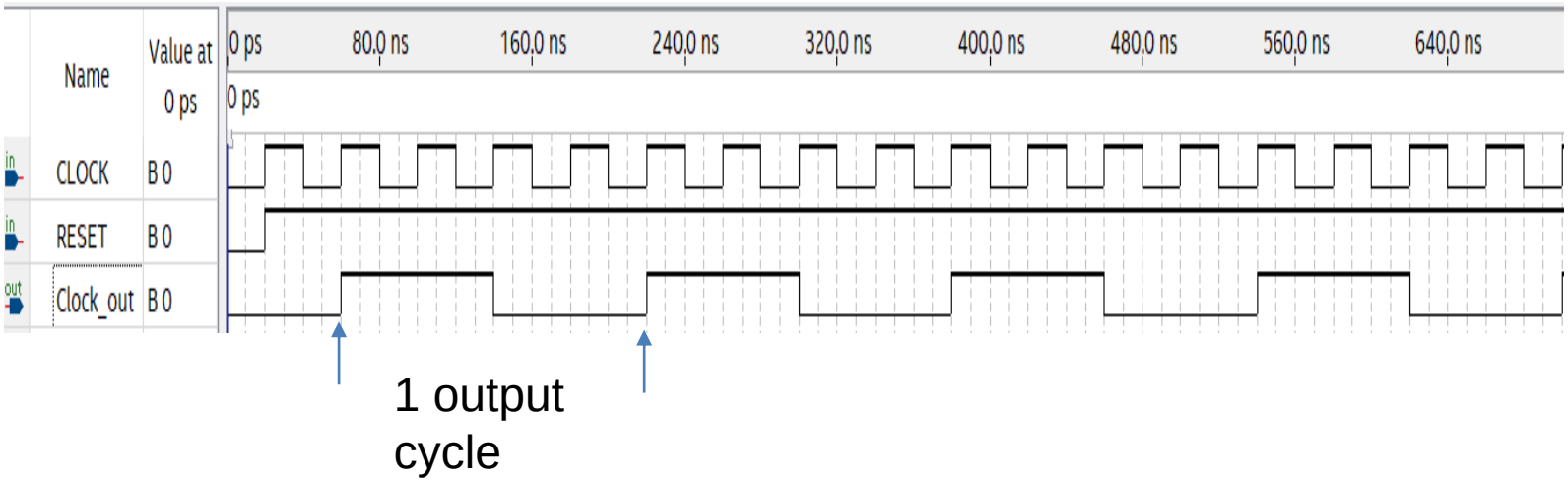
- Sequential circuits with practical applications often require a clock much slower than the internal clock of DE-10 board.
- Important terms/concepts include:
  - Clock or frequency division
  - Multi-process architecture
  - Seven segment LEDs

Clock or Frequency Division

- A circuit with practical application often requires clock frequency much slower than the clock available in DE-10 board. For example, a digital watch displays numbers in every second, that is a clock frequency of 1 Hz is needed.
- To divide a frequency, f by N to get a new frequency fnew, then the relationship can be written as:
- N= f/fnew, where N is known as scaling factor.
- Thus to divide 25 MHz with a scaling factor of 4,

Clock or Frequency Division

- Figure is showing a divided clock derived from 25 MHz with a scaling factor of 4 and the output frequency is 6.25 MHz.
- Note that each output clock cycle has 4 cycles of 25 MHz clock- 2 cycles for high and 2 cycles for low for 50% duty cycles output clock.



Clock Division using VHDL

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;
ENTITY clock_div IS
PORT ( CLOCK, RESET: IN  STD_LOGIC;
          CLOCK_OUT:  OUT  STD_LOGIC);
END clock_div;
ARCHITECTURE behavior OF clock_div IS
SIGNAL COUNT: INTEGER:=1;
SIGNAL TEMP_CLOCK : STD_LOGIC := '0';
 BEGIN
```

This library component will allow to use both signed and unsigned numbers and allow to use arithmetic operations like addition, subtraction etc on numbers.

--Here CLOCK is the original clock frequency and CLOCK_OUT is the divided clock frequency.

Clock division in VHDL: Continue

```
PROCESS (CLOCK, RESET)
BEGIN
IF (RESET = '0') THEN
COUNT <= 1;
TEMP_CLOCK <= '0';
ELSIF (RISING_EDGE (CLOCK)) THEN
COUNT <= COUNT+1;
IF (COUNT = 2) THEN
TEMP_CLOCK <= NOT (TEMP_CLOCK);
COUNT <= 1;
END IF;
END IF;
END PROCESS;
CLOCK_OUT <= TEMP_CLOCK;
END behavior;
```

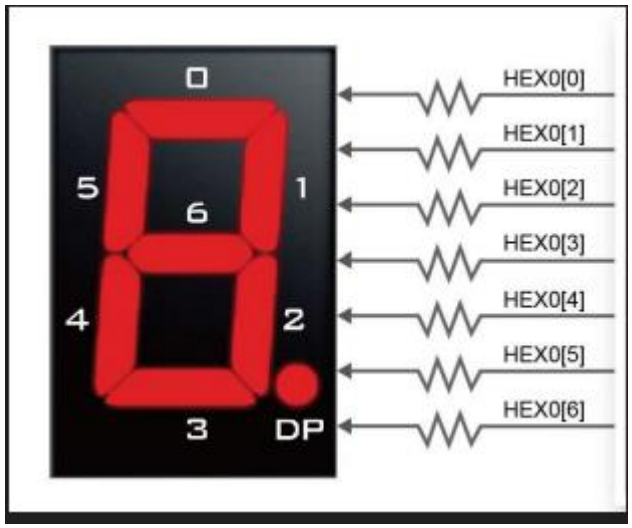
TEMP_CLOCK is the new clock that is created by inverting in every 2 cycles of the original clock is counted. The scaling factor in this example is 4.

Seven Segment LED

Seven segment LED displays are often found in digital clocks, calculator, many other home appliances to list a few.

They are primarily used to display decimal numbers, but they can also display a few alphabets and other characters.

Some 7-segment LEDs also provide a circular LED for decimal point display



DE-10 has a total of six 7-segment LEDs and the most right one on the board is designated as HEX0 which is used as vector with size 7. The top segment of HEX0 is HEX0[0] which is numbered as 0, the top right one is HEX0[1] which is numbered as 1, and so on.

Programming seven segment

- The LEDs in seven segment display can be arranged with a common anode or common cathode configuration.
- For a common cathode, the cathodes of all seven segments LEDs are tied together and connected to the ground. A logic ‘1’ is applied to the segments that need to be turned on.
- In common anode displays, all the anodes are tied together, and the common anode is connected to the supply voltage. Individual segments are turned on by applying logic 0 to their cathodes.
- DE-10 standard board uses common anode and thus individual segments can be turned on by providing ‘0’ to them.
- For example, to display number 1, the segment 1 (hex0[1]) and 2 (hex0[2]) need to be set at low or ‘0’ logic whereas the other segments need to be set at high or ‘1’.

Lab 7 Deliverables

- Lab 7 Prelab
  - Draw the state diagram of modulo 10 up/down counter .
  - Simulation of modulo 10 counter
- Lab 7 Work
  - Implement modulo 10 counter in DE-10 board
  - Use of the 7-segment LEDs to display numbers from 0 - 9

Lab 7 Deliverables

- Lab 7 results
  - State diagram of modulo 10 up/down counter
  - Functional simulation results for the design.
  - VHDL codes of modulo 10 up/down design form the lab
  - A picture of the DE-10 board displaying a number