ENGR 2323 Digital Design Lab
Combinational Circuit Propagation Delay

Propagation Delay

The propagation delay is the time from when the input of a device changes to when output of the device changes. We typically are interested in the worst-case propagation delay; the delay along the longest combinational delay path from input to output. Propagation delays are typically measured from 50% of the input level to change to 50% of the output level change.

Consider determining the worst-case propagation delay for the circuit of Figure 1 that realizes the MSOP

$$Y = A \cdot B + \overline{C} \cdot \overline{D} + \overline{A} \cdot C \cdot D$$

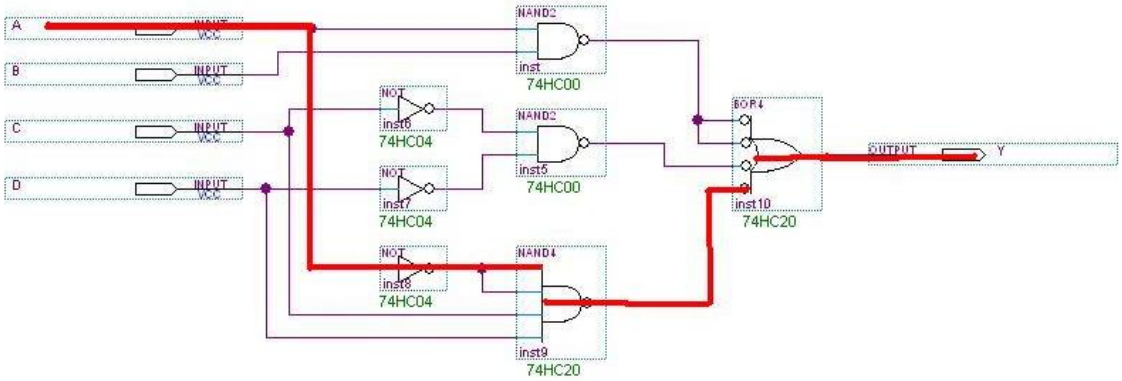

Figure 1. Circuit for Propagation Delay Example

Note: this example uses devices from the HCT family whereas the ENGR 2323 chips are from the LS family. Make sure to use the correct datasheet to get the device delays.

Using the data sheet tables (like in Figures 2a and 2b) and assuming Vcc = 4.5 Volts and ambient temperature of 25 degrees Celsius, we obtain the worst case propagation delays for each device in the circuit.
74HCT00 (2-input NAND): 25ns
74HCT04 (inverter): 25ns
74HC20 (4-input NAND): 28ns

The maximum propagation delay (input to output) is for A to Y (A – NOT – NAND4 – bOR4 – Y),
Maximum Propagation Delay = 25ns + 28ns + 28ns = 81ns

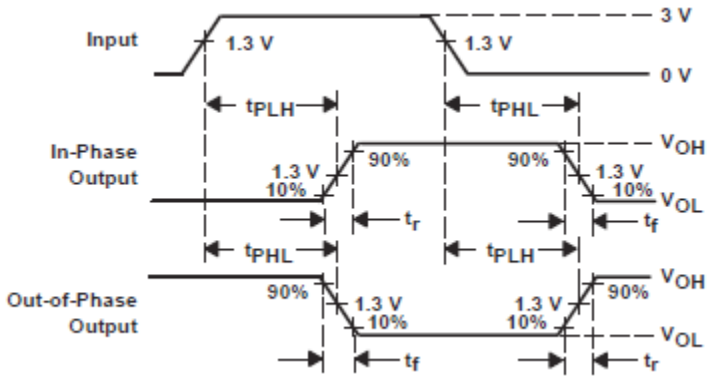

Figure 2a. Voltage Waveforms, Propagation Delay and Output Rise and Fall Times, Texas Instruments SN74HCT00 Data Sheet

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT00		SN74HCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		11	20		30		25	ns
			5.5 V		10	18		27		22	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

Figure 2b. Switching Times for SN74HCT00, Texas Instruments SN74HCT00 Data Sheet

Input Combinations for Measuring Propagation Delay

The input changes corresponding to the maximum delay path can be measured by setting all the values except the input corresponding to the maximum delay path to set values, changing the input corresponding to the maximum delay path, and then measuring how long it takes from the input changing to the output changing.

To determine what the values other than the input corresponding to the maximum delay path are we need to identify two rows in the function table with different outputs and whose inputs differ in only one bit position, that of the signal corresponding to the maximum delay path. It is not as simply as just identify two rows that differ in the bit position because if the input has more than one path to the output, we need to ensure the rows correspond to the maximum delay path.

The function table for the circuit of Figure 1 is given in Figure 3. The rows corresponding to the maximum delay path are shaded. The process for identifying these rows is as follows:

First apply propagating values at all inputs of gates except the A input (A is the signal to be propagated in this example). These values are shown in Figure 4a. Propagating values pass a signal or its complement to the output of the device and controlling values fix the value of the output of the device. For NAND and bOR gates, 0s on any input fixes the output at 1 and 1s on all the inputs except one propagates the complement of the other input line (1s are propagating values for NAND and bOR gates and 0s are controlling values).

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 6. Truth Table for Maximum Delay Path Example

After applying the propagating values to propagate A, two of the input values for the maximum delay path are known. C and D must both be 1 to propagate A through the NAND4.

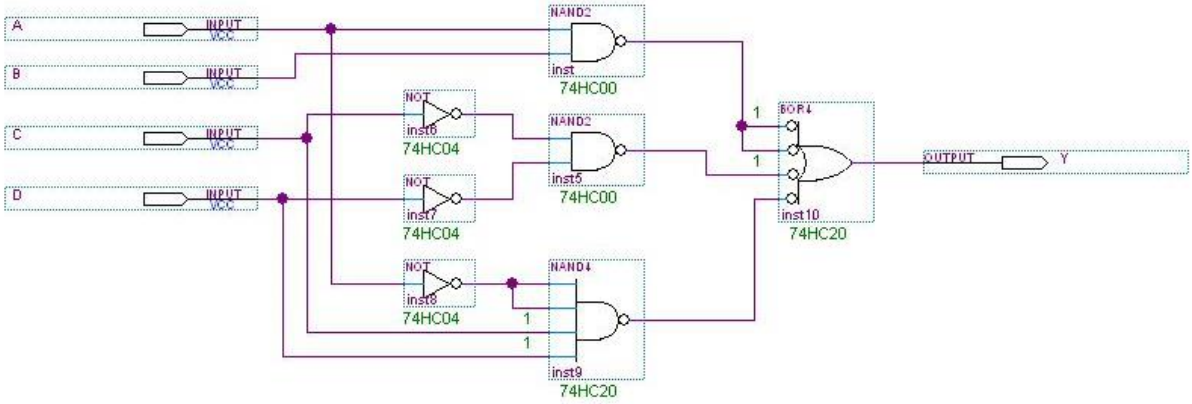

Figure 4a. Propagating Values for A Input

Next, determine any remaining input values by assigning the appropriate propagating or controlling value to get the correct signal values set previously. With C = 1 and D = 1, the inputs of the second NAND2 are both 0s which will give a 1 output which matches the propagating value set previously. To get a 1 as the output of the first NAND2, we need at least one of its inputs to be a 0 and since we cannot set A, the propagating signal to 0, B must equal 0. The result of this is given in Figure 8b. The input values other than A corresponding to the maximum delay path are B = 0, C = 1, and D = 1. This corresponds to rows three (0011) and eleven (1011) in the function table.

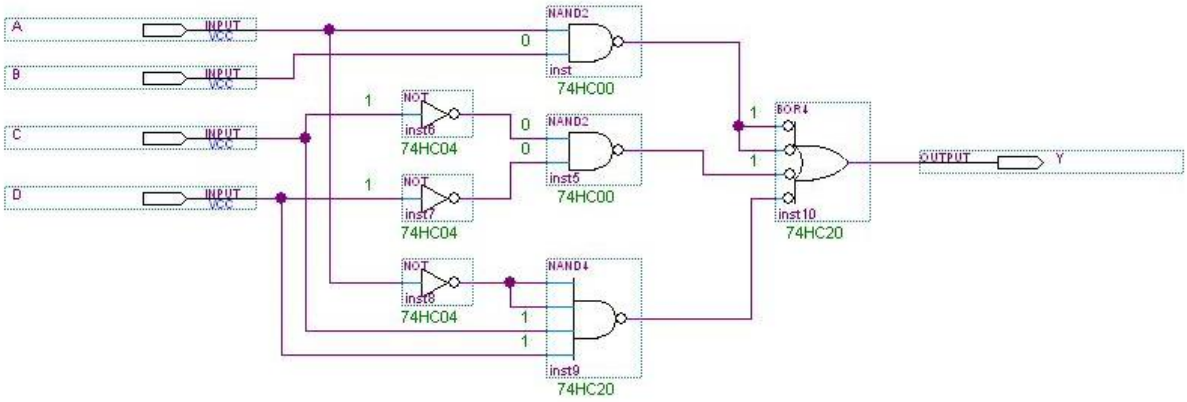

Figure 4b. Propagating and Controlling Values to Propagate A to Output Along Max Delay Path

References

None

Last modified Thursday, August 25, 2022