Lab 4

ENGR 2323

Digital Design Lab

Class Outline

- Digital circuit timing.
- Oscilloscope measurements.
- Datasheets.
- Combinational circuit delay paths.
- Measuring Propagation Delay on Constructed Circuit.
- Lab 4 deliverables.

Objectives

- Be able to obtain timing information from integrated circuit manufacturer datasheets.
- Be able to reset an oscilloscope to its default settings and verify its calibration.
- Be able to determine the period and duty cycle of a periodic signal.
- Be able to determine the worst-case propagation delay of a combinational circuit.
- Be able to analyze the timing of digital circuits with an oscilloscope.

Important Terms/Concepts

- Digital circuit timing is important for determining the delay for a circuit output once an input is applied and for determining maximum clock rates circuits can be run at.
- Worst case digital circuit timing can be determined using the timing information from manufacturer datasheets. The actual digital circuit timing can be determined using bench equipment such as a mixed signal oscilloscope and logic analyzer.
- Important terms/concepts include:
  - Worst case delay, worst case delay path
  - Period, duty cycle
  - Rise time, fall time, propagation delay

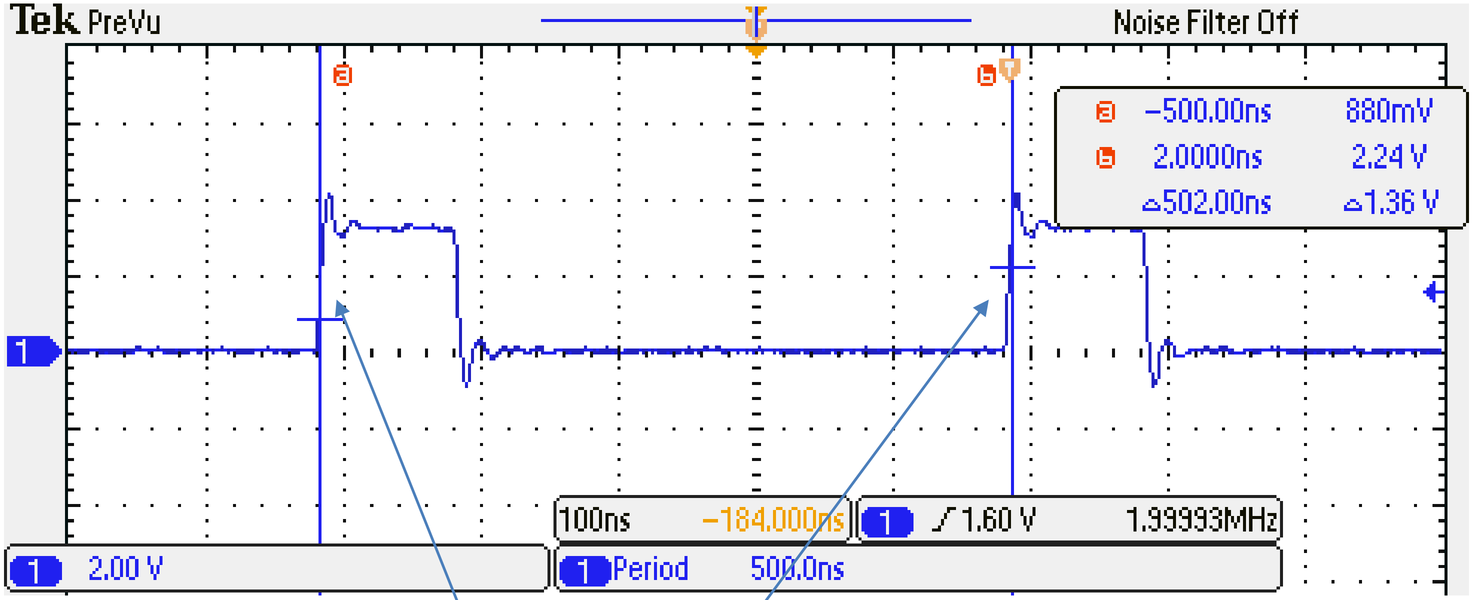
Design Circuit Timing

- Digital circuit timing may involve measuring the following: period, duty cycle, rise and fall times, and propagation delay.
- The period of a signal is the smallest time for which the signal repeats itself.
  - Measured for square/rectangular wave type signals.
  - Measurement taken from 50% of rising edge of to 50% of next rising edge.
- The duty cycle is the percentage of time in the period the signal is high; time high divided by the period. Duty cycle gives an idea of how much energy the signal uses in one period, more time high the more energy.
  - Measure the period.
  - Measure the width of the time high from 50% of rising edge to 50% of falling edge.
- The rise time is the time it takes for a signal to get from 10% to 90% of its settling values. The fall time is the time it takes for a signal to get from 90% to 10% of its settling values.
  - Measure time from 10% of rising edge to 90% of rising edge (or 90% to 10%).
- The propagation delay of a circuit is the time from when the input of a device changes to when output of the device changes (50% to 50%).
  - Measure from 50% of input edge to 50% of output edge.

Oscilloscope Measurements

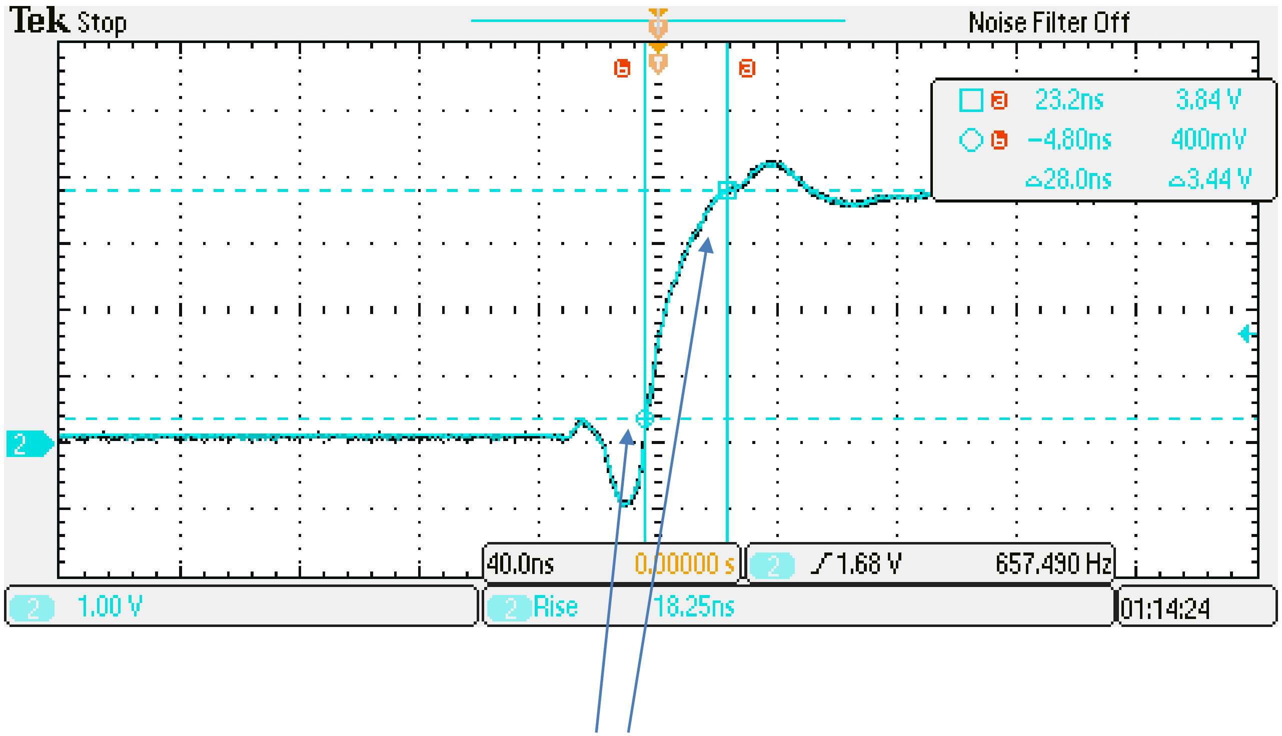
- Modern digital oscilloscopes allow signal measurements to be taken automatically (choose desired measurement form menu) or using cursers.
- Tektronix MSO 2002B has two horizontal and two vertical cursers which can be placed to locate measurement points.
- Oscilloscope will compute a Δt for vertical cursers or ΔV for horizontal measurements. The Lab 4 measurements (period, rise/fall time, propagation delay) are all Δt measurements. You can place the horizontal cursers at the voltage value (10%, 50%, 90%) and then use the vertical cursers to measure the Δt.
- Any time you use an oscilloscope verify the settings. For ENGR 2323 lab since many people use the same scope, always rest the oscilloscope before taking measurements.

Period Measurement



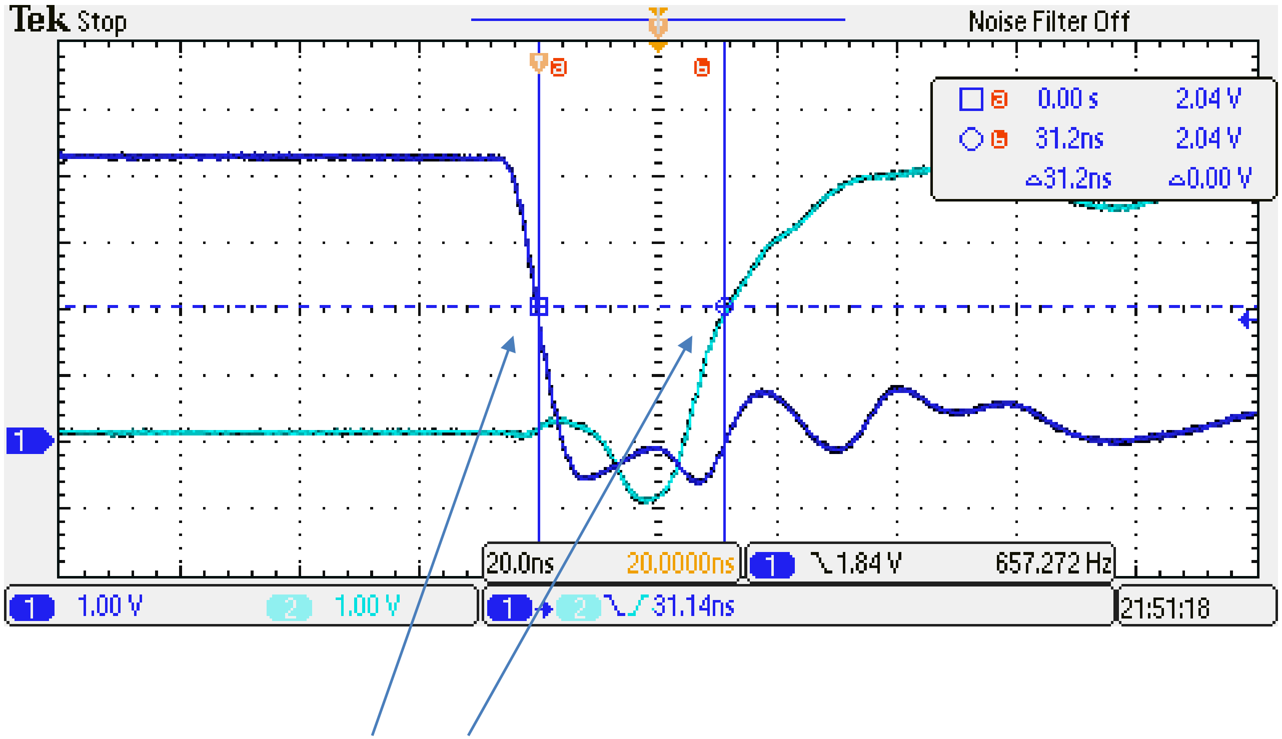
50% rising edge to 50% next rising edge

Rise Time Measurement



10% rising edge to 90% rising edge (notice that the settling value not peak from the under or overshoot is used for 0% and 100% values).

Propagation Delay Measurement



Input change of H to L causes output change of L to H. This is L to H delay (named based on output change). For this example, 50% of falling edge of input to 50% of rising edge of output.

Datasheets

- You will need datasheets for the following discrete logic chips: 74LS00, 74LS04, and 74LS20.
- These devices were used to realize your lab 3 design and you will need the worst-case delay for each of the devices.
- For the circuit timing you look at the timing/switching characteristics (t_{PLH}, t_{PHL}).

SN74LS00 Datasheet

6.9 Switching Characteristics: SNx4LS00

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ and C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

6.11 Typical Characteristics

C_L = 15 pF

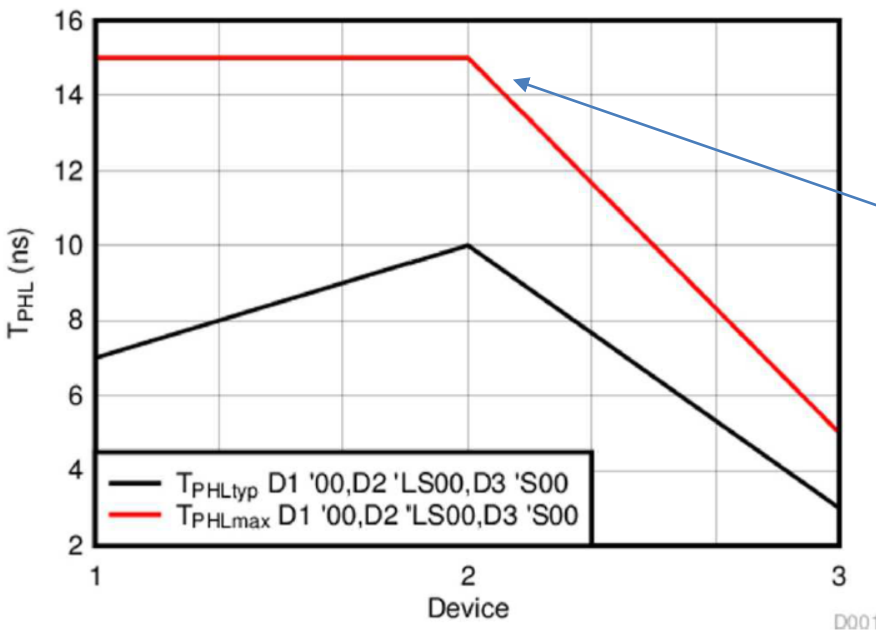


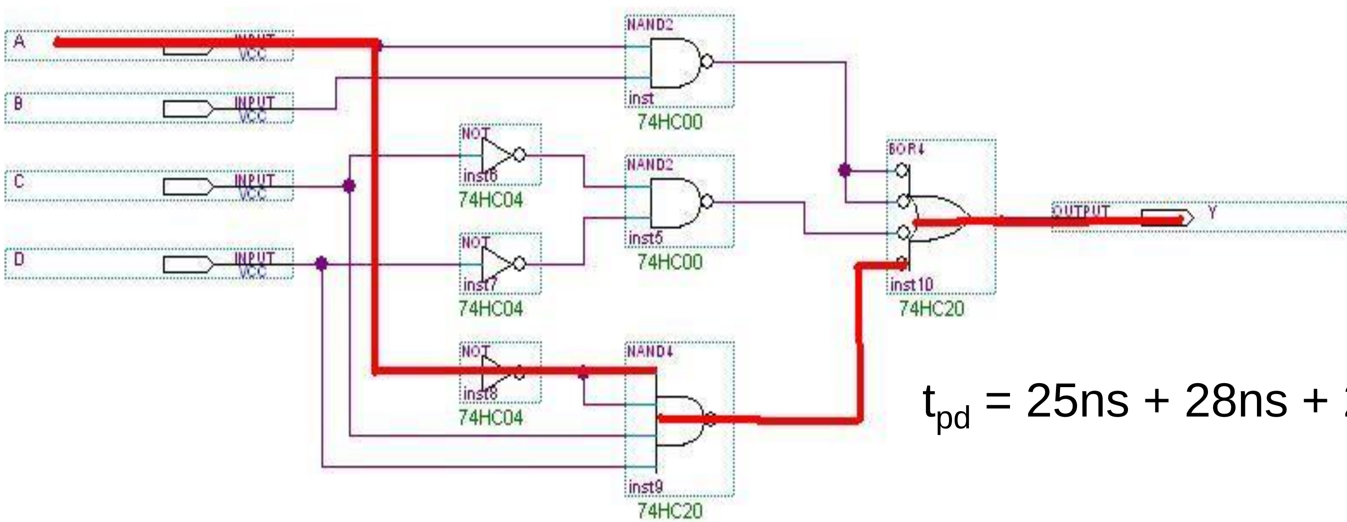
Figure 1. T_{PHL} (Across Devices)

For V_{cc} = 5V, ambient temperature 25C, max t_{PLH} and t_{PHL} are both 15ns. So worst case delay for this device is 15ns.

Combinational Circuit Delay

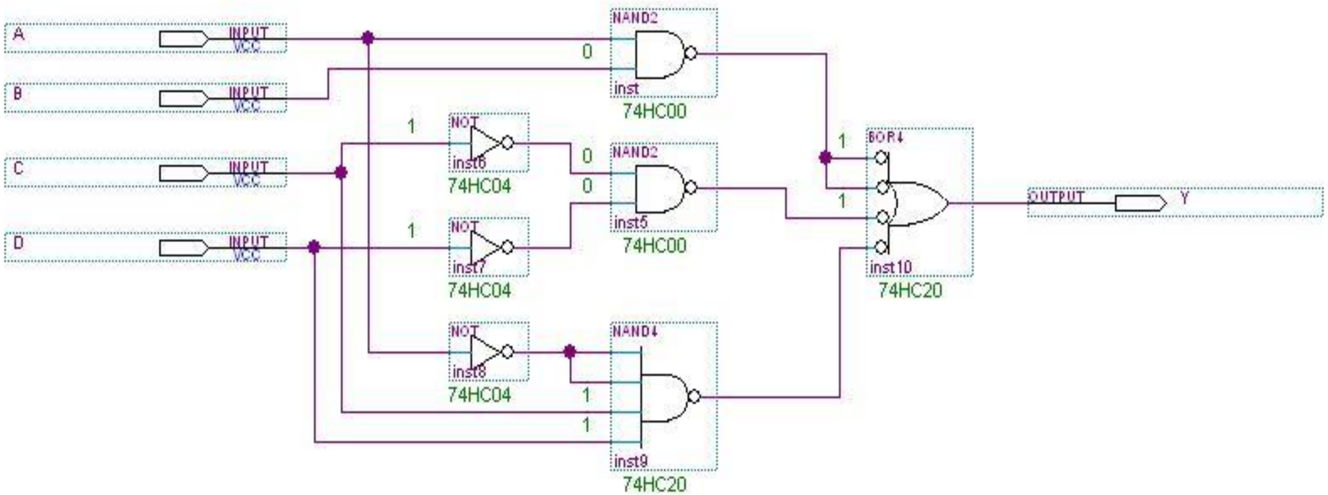
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^0C$ MIN	TYP	MAX	SN54HCT00 MIN	MAX	SN74HCT00 MIN	MAX	UNIT
t_{pd}	A or B	Y	4.5 V		11	20		30		25	ns
			5.5 V		10	18		27		22	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

Using the data sheet tables and assuming Vcc = 4.5 Volts and ambient temperature of 25C, worst case device delays
74HCT00 (2-input NAND): 25ns ,74HCT04 (inverter): 25ns, 74HC20 (4-input NAND): 28ns



t_{pd} = 25ns + 28ns + 28ns = 81ns

Worst-case Delay Path



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Propagating values for a NAND/bOR gate are 1s
Controlling values for a NAND/BOR gate are a 0, 0 on input sets output to 1

The maximum propagation delay (input to output) is for A to Y (A – NOT – NAND4 – bOR4 – Y),
t_{pd} = 25ns + 28ns + 28ns = 81ns

Measuring Propagation Delay on Constructed Circuit

- Using the two rows corresponding to worst case delay path:
  - One input value in the pair of rows is different, the other three input values are the same in both rows.
  - Set three of the powered protoboard switches to the values that are the same for the two rows.
  - The remaining input will be provided by a square wave (TTL square wave from CADET board of around 100 Hz). The output will then be changing back and forth from 0 to 1.
  - Channel 1 probe should be connected to input (100Hz square wave) and Channel 2 to output (signal going to LED).

Lab 4 Deliverables

- Lab 4 Prelab
  - Table of worst-case propagation delay for each of the integrated circuits in the circuit.
  - Annotated Quartus schematic including device names, pin numbers, and worst-case propagation delays. Indication of the maximum delay path from input to output for the circuit and the value of the maximum propagation delay.
  - Function table with pair of rows corresponding to the worst-case delay path from input to output highlighted.

Lab 4 Deliverables

- Lab 4 Work
  - Perform an oscilloscope reset.
  - Reconnect the circuit constructed for lab 3 and verify its operation.
  - Set three of slide switches to values from pair of rows in function table and remaining the remaining input should be disconnected from switch and connected to 100Hz square wave.
  - Measure period and duty cycle of input connected to square wave. Save screenshots of each measurement.
  - Measure rise and fall time of circuit output. Save screenshots of each measurement.
  - Measure low to high and high to low propagation delays. Save screenshots of each measurement.

Lab 4 Deliverables

- Lab 4 Results
  - Annotated Quartus schematic including device names, pin numbers, and worst-case propagation delays. Indication of the maximum delay path from input to output for the circuit and the value of the maximum propagation delay.
  - Function table with pair of rows corresponding to the worst-case delay path from input to output highlighted.
  - Oscilloscope screen captures showing period and duty cycle measurements (and the measured values) of the square wave signal.
  - Oscilloscope screen captures showing rise time and fall time measurements (and the measured values) of the circuit output signal.
  - Oscilloscope screen captures showing worst-case propagation delays (and the measured values) for the circuit.
  - Comments on how the measured propagation delays compare to the maximum propagation delay of the circuit determined using the data sheet values.