The step numbers in this data sheet refer to those in the laboratory exercise instructions.

Steps 2 through 4:

Table 2. MOSFET Model Q-Points, *G*M and *r*o values.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Model Name | Q-Point *V*DS (V) | Q-Point *V*GS (V) | Q-Point *I*D (mA) | DC *G*M (mS) | Output Conductance | Output Resistance *r*o |
| NMOS1 | 5.0 | 3.5 |  |  |  |  |
| PMOS1 | −5.0 | −3.5 |  |  |  |  |
| PMOS2 | −5.0 | −3.5 |  |  |  |  |

Steps 5 and 6:

Table 3. CMOS Inverter Input Logic Level Threshold Voltage

|  |  |
| --- | --- |
| Inverter Circuit | Logic Level Threshold Voltage |
| NMOS1-PMOS1 |  |
| NMOS1-PMOS2 |  |

Step 7:

Table 4. Inverting Amplifier Maximum Gains and Input Range

|  |  |  |
| --- | --- | --- |
| Configuration | Maximum Gain | Input Range for Max Gain |
| Closed-loop |  |  |
| Open-loop |  |  |

Other observations: